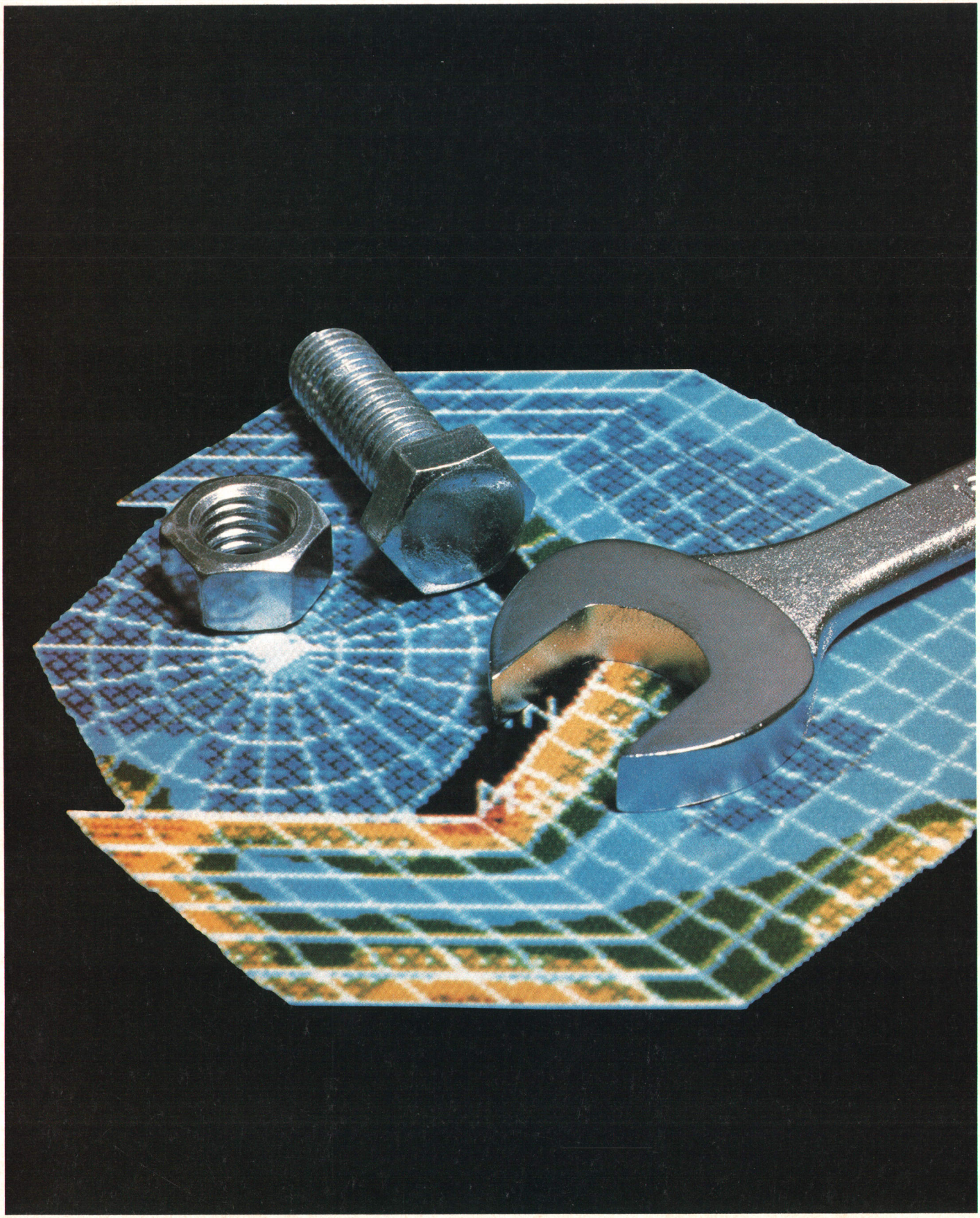
HEWLETT-PACKARD
JOURNAL

MAY 1984

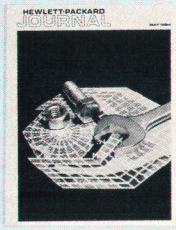


HEWLETT-PACKARD JOURNAL
Technical Information from the Laboratories of Hewlett-Packard Company

MAY 1984 Volume 35 • Number 5

Contents:

In this Issue:



This issue wraps up the design story of the HP 9000 Series 500 Computers, Hewlett-Packard's new 32-bit machines based on the advanced technologies for integrated and printed circuit production that were featured in our August 1983 issue. The five very large-scale integration (VLSI) chips used in these computers, including the 450,000-transistor central processing unit (CPU) chip, are produced using HP's proprietary NMOS-III integrated circuit process. Mounted directly on copper-cored boards called finstrates, these chips are the basis for three kinds of functional units—CPU, input/output processor, and memory—that can be housed in various combinations in a compact Memory/Processor Module. In the HP 9000 Model 520, the desktop workstation member of this computer family, this technology can give an individual scientist or engineer exclusive use of the processing power of a large mainframe computer for such computation-intensive tasks as finite element analysis (see cover). Models 530 and 540 offer the same technology in rack-mount and cabinet versions that can be built into systems and/or shared by several users. Model 520 offers a choice of operating systems—HP BASIC or the UNIX-like HP-UX. Models 530 and 540 offer only HP-UX. Two months ago, our March issue was devoted to the operating systems and other system software for these computers. This issue focuses more closely on the three Series 500 models. The articles on pages 3 and 12 deal with the engineering that was done to incorporate the Memory/Processor Module into the Model 520 desktop workstation and give it a color graphics display. The graphics and input/output features of Model 520's BASIC language are explained by the designers in the articles on pages 16 and 21. The hardware design story of the Model 530 and 540 Computers begins on page 31, and the power supply design for all three models—unusually difficult because of the 520's compactness—is the subject of the article on page 24.

On the subject of finite element analysis, both third-party and HP software packages for this complex art will be available for the HP 9000 Model 520 in the next few months. The HP finite element package will run on HP 9000 Series 200 Computers as well, but is faster on the Model 520.

-R. P. Dolan

Putting a 32-Bit Computer System in a Desktop Workstation

A modular packaging approach provides a powerful computer workstation for computer-aided design and engineering applications.

by Jack L. Burkman, Robert L. Brooks, Ronald P. Dean, Paul F. Febvre, and Michael K. Bowen

AS COMPUTER TECHNOLOGY evolves, the hardware offered to users for a given cost decreases in size and/or increases in complexity. One result of this evolution is Hewlett-Packard's most powerful desktop computer system—the Model 520 of the HP 9000 Series 500 Computers (Fig. 1).

Made possible by HP's proprietary NMOS-III VLSI technology,[1] this workstation provides engineers and designers with a personal 32-bit computer system capable of performing many of the CAD (computer-aided design) and CAE (computer-aided engineering) applications normally requiring a large mainframe computer system. The heart of the Model 520 is the 32-bit HP 9000 Series 500 Memory/Processor Module,[2] a twelve-slot card cage for holding various user-selected combinations of CPU cards (up to three), I/O processor cards (up to three), and 256K-byte RAM cards. In addition, the Model 520 contains a variety of peripherals:

- A high-speed thermal printer
- A 10M-byte hard-disc mass memory
- A 5¼-inch flexible disc drive
- Up to five high-performance I/O channels for connecting additional peripherals
- A keyboard
- A choice of three CRT display options.

A sophisticated operating system kernel, called SUN,[3] coordinates the operation of this hardware and provides an interface to high-level systems such as HP-UX[4] (an enhanced version of UNIX™) and BASIC (see reference 5 and articles on pages 16 and 21).

Each part of the Model 520 conducts its own self-test when the machine is turned on. Any failures are indicated by appropriately lighted LEDs (light-emitting diodes) on each module and the operating system logs the failures, displays them on the CRT, and configures the Model 520 to operate around them, if possible. If the display fails, the

UNIX is a U.S. trademark of Bell Laboratories

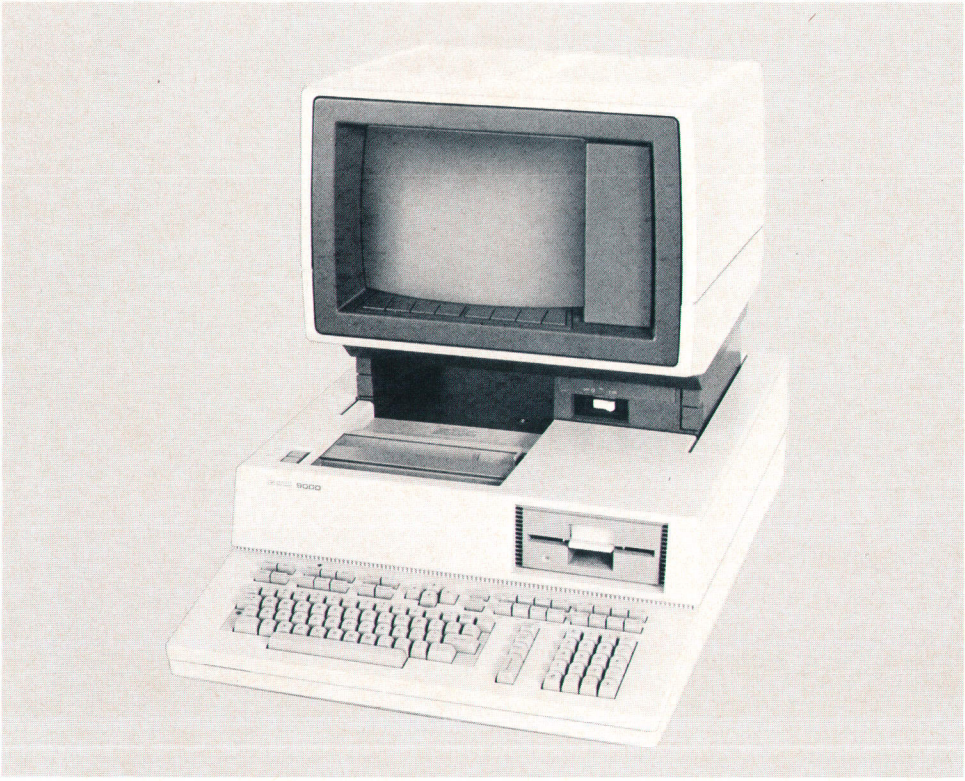


Fig. 1. *The HP 9000 Model 520 Computer is a 32-bit computer system based on HP's NMOS-III VLSI and finstrate technologies.It provides professional personnel with a desktop workstation having mainframe computer capabilities. The Model 520 contains its own printer, hard and flexible disc memory devices, I/O processor, and keyboard. Several CRT display options are available. The Model 520 can have up to three CPUs for increased performance in computation-intensive applications or up to 2.5 megabytes of RAM for data-intensive work. For I/O-intensive work, up to three I/O processors can be installed.*

printer is used to report the failures. If the Model 520 is connected in a multiuser HP-UX system, the failures are also reported on the system console.

If any portions of the memory cards are bad, the failed portions are blocked out and the amount of memory loss is reported to the display. In addition, during normal system operation, the operating system continually tests the memory for soft errors at a rate of 12 megabytes/day as a background function. Single-bit errors are corrected; double-bit errors are detected and reported.

Careful design and a special power supply (see article on page 24) were necessary to fit this computer system into an enclosure small enough to sit on a desktop. This package had to satisfy the basic ergonomic requirements of the operator and provide adequate cooling for all the electronic components, while remaining manufacturable and serviceable. To understand the product design challenge, consider some of the Model 520's characteristics. The total amount of power dissipated inside the enclosure approaches one kilowatt, a fully loaded machine weighs over 70 kilograms, and the ac line filter volume required measures over 820 cubic centimeters.

Modular Design and Assembly

The design of the Model 520 is founded on the concept of independent modules linked together to form a highly compact package (Fig. 2). This approach allows each module to be tested fully by itself before assembly. A structural foam base (Fig. 2a) reinforced with two aluminum die castings and a central sheet-metal "bucket" forms the structure for mounting the modules. A multilayer printed circuit board, two ribbon cables with connectors, and a fan wiring harness are added to this basic structure to connect the modules electrically (Fig. 2b).

The Memory/Processor Module containing the CPUs, I/O processors, and RAM has its own cooling fan and is sealed to prevent electromagnetic interference (EMI). This module is inserted into the left rear chamber of the base assembly, and requires only the installation of the fan cable, internal I/O (input/output) cable, and eight screws. The I/O back-

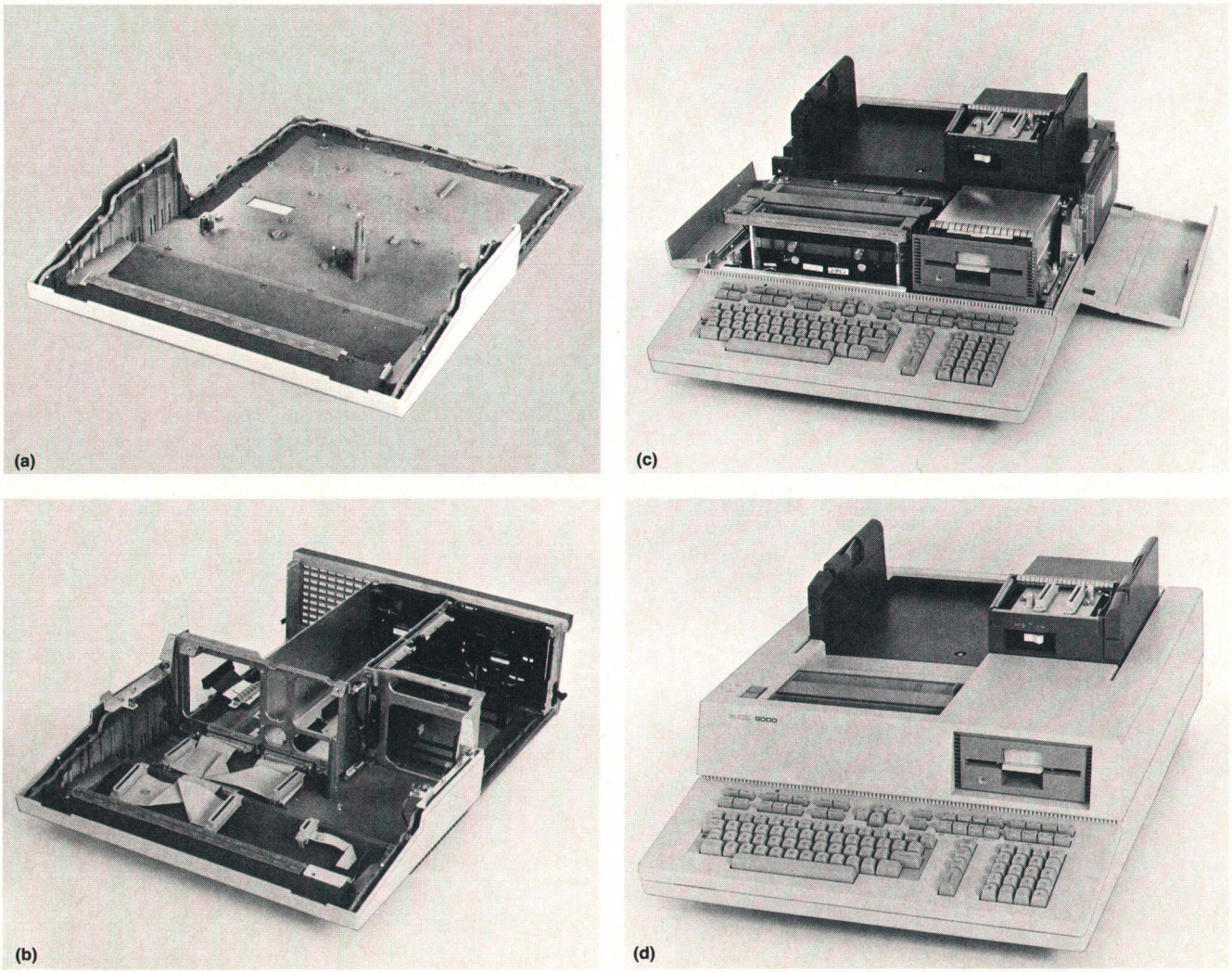


Fig. 2. *Packaging of the Model 520 Computer begins with a structural foam base (a) to which is added a sheet-metal "bucket," two aluminum die castings, a printed circuit board, and wiring harnesses (b). The various modules are then inserted (c) and the covers are put on (d).*

plane board and two card guides are attached to the inside of the right rear chamber, and with the ac line filter module and a metal door, form the I/O and mass memory controller card cage. The line filter module houses the circuit breaker and ac line filter. It is placed on the top of the right rear chamber and installed with four screws. The power supply module is inserted into the center rear chamber. The ac line from the line filter module is coupled to the power supply and four captive fasteners are tightened to secure the assembly. The printer module is installed into the space directly in front of the processor and power supply modules and is secured with two captive fasteners. The mass memory modules are located directly in front of the I/O card cage. These devices require the attachment of dedicated cables to their controller boards and the tightening of three captive fasteners. The last module installed (Fig. 2c) is the keyboard, which uses four captive fasteners. Each module can be removed independently. Each module is also fully guided during installation to ensure proper connector alignment.

The covers (Fig. 2d) provide more than a clean appearance and EMI suppression. The rear cover provides access to the ac line circuit breaker from the front of the machine and houses the printer paper tray and the tilt mechanism supporting the CRT display. The front cover allows access to the power supply module's diagnostic LEDs (light emitting diodes) without turning the machine off. It also allows the mass memory devices and printer to be accessed without removing the CRT display. All screws used to attach both of these covers are captive. These features greatly reduce the time needed to access the interior modules for service.

The side access doors, base reinforcement strips, and keyboard cover are installed last. The keyboard cover snaps into position over the keyboard. The base reinforcement strips snap onto the left and right rear sides of the base and two screws on each strip are tightened to provide the required structural strength. These strips allow easy access to the bottom of the processor module and the I/O card module when removed. The side access doors, which also snap into position, provide access to the processor, I/O, and mass memory diagnostic LEDs without turning the machine off. They also provide easy access to the processor module cards and the I/O cards.

An external interface module was designed to allow the use of earlier HP 9845 Computer CRT displays for the Model 520. This interface is attached to the CRT display assembly and the assembly is placed on the two pedestals on top of the rear cover. Installation of the display also completes the electrical connection to the Model 520's base automatically.

System Cooling

The high level of integration and performance in the Model 520 presented the packaging challenge of dissipating a heat load of approximately 900 watts. High reliability is achieved by maintaining device junction temperatures at levels significantly less than the maximum value specified by the device manufacturer. Under worst-case conditions, the temperatures inside the Model 520 do not exceed 80% of the maximum junction temperature specification. These worst-case conditions occur when the machine is fully loaded and operated in a 40°C ambient temperature at 4570 m elevation. The 40°C temperature limit is imposed by the mass storage media. The other modules are designed for reliable operation up to 55°C. The I/O cards are inside the machine, where forced-air cooling allows these high-performance cards to maintain reliable operation even at 55°C. In a typical environment of 25°C at sea level, component temperatures are maintained at approximately 50% of the maximum junction temperature.

The results of early tests dictated the creation of a large inlet plenum and three air flow chambers for the Model 520. This arrangement equalizes the air volume flowing through the processor, power supply, I/O, and mass memory modules. Two broad inlets reduce the pressure drop through the inlet screen and provide cooling along the entire length of the keyboard. The printer heat load is distributed equally between the air supplies for the power supply and the processor modules. An aluminum die-cast

(continued on page 7)

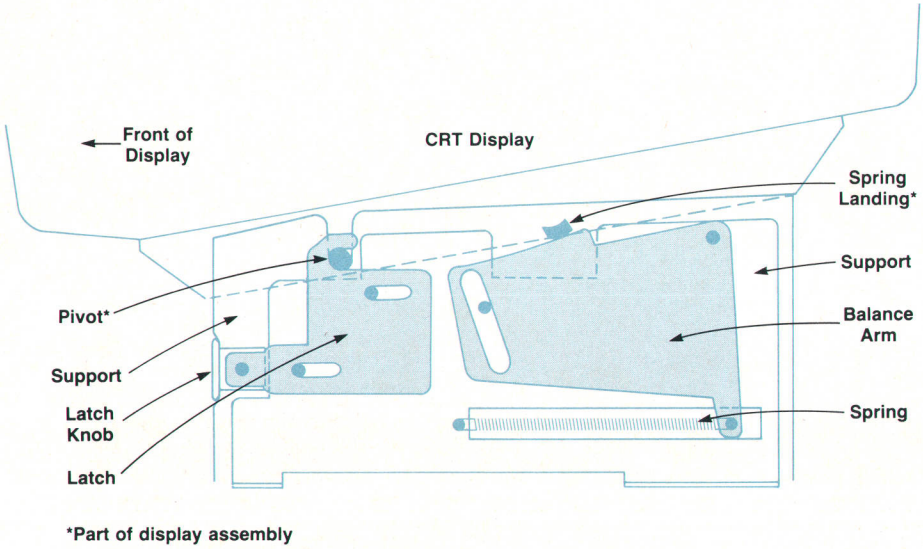


Fig. 3. *CRT display tilt mechanism located inside each of the two pedestals on top of the rear cover of the Model 520 (see Fig. 2d). This design adapts to different CRT display option weights by simply changing the position of the spring-landing part fastened to the display.*

Low-Tech Modeling for Better Design

Design is an iterative process. Mother Nature, the grand designer of all time, is still trying out new models and variations on basic designs that have been in production for thousands and millions of years. Each new version is submitted to rigorous testing. The ones that pass are approved for further production, the failures fade away.

It isn't really that much different when humans design, except that they generally operate on a different time scale, which at HP is called a schedule. In the case of a product like the HP 9000 Model 520 Computer, the time scale was measured in months. About 60% of those months were spent deciding what the product was going to be: what its component parts would be, how big it should be, what it should look like, etc. Then there was an intense period of several months in which the actual design of the product package was accomplished.

The major objective of this period was to convert the images of various parts in various designers' minds into actual hardware that could be manufactured, assembled, tested, sold, and serviced. Making more than one of something invariably leads to mass-production techniques such as tooling. This presents a severe schedule and cost constraint all by itself, for the tool for a part like the structural foam base of the Model 520 took weeks to design and build, and was expensive. The Model 520 has five major structural foam parts, four die castings and a couple of dozen miscellaneous tooled plastic parts. All of the tools for these parts took time to produce and cost money, which meant that we really wanted to do it right the first time. So there was our fundamental challenge: achieving sufficient iterations of the design early enough to have high confidence that the first tooled parts would be correct.

A few words about the design process—a product designer at HP is responsible for conceiving and defining the physical parts used in the product. Many are standard parts that we purchase from vendors or are used in other HP products—screws, connectors, cables, electronic parts, etc. But others we design specifically for one product, and in the case of an integrated desktop computer like the Model 520, this included the case parts plus most of the structural parts inside. Conceiving each part is one phase—deciding what it must do and how best to accomplish the task, and considering the many alternatives at each step. Documenting the solution is another phase, and the basic 3-view mechanical drawing is still the primary document that directs other people in producing the part.

The Model 520 is not a simple product, and the odds were extremely slight that each member of the design team would be able to sit at the drawing board and create drawings of parts, and that all of these parts would fit together properly. It is a big enough challenge to visualize and draw one part, let alone hundreds of interconnected ones. So we were after a way to let the design team visualize, make mistakes, and improve the designs until we got what we wanted, and then to make the tools with some confidence that they would be right the first time.

The technique we used was modeling, which is common enough. The different twist was that we did not go high-tech with expensive, complex, computer-aided three-dimensional drafting, but went low-tech with foam-core board (a styrofoam and paper form of cardboard), sharp knives, and hot-melt glue. Despite this unsophisticated approach, the increase in our productivity was on the order of 20 to 40 times in the crucial early design phase where iteration is so important.

That sounds like an unbelievable increase, but it is easy to demonstrate. Usually a designer first makes mechanical drawings of a new part. Then to verify the design, the designer sends the drawings to a model shop to have one or two parts made. If this traditional approach had been used for the Model 520 design, the time involved for a typical part might have been a couple of days on the drawing and then several days in the model shop.

However, a serviceable foam-core mockup (a 3-D sketch) could be made in an hour or two, fitted to other parts, and modified in minutes if necessary. The feedback was almost immediate, and the effort required to change things was so slight that the process almost encouraged us to build the part again. So we could have two iterations in 2 to 4 hours, while the model shop approach might take 40 to 80 hours. For the more complex parts, creating the mockup first was the quickest way for the designer to visualize the part before doing the initial drawing, saving days or weeks of drawing time.

The first drawings were only rudimentary layouts, trying to obtain the best machine configuration in terms of cooling airflow, ergonomics, accessibility, serviceability, etc. Many of the component modules were already well-defined in terms of size and shape—the Memory/Processor Module, the thermal printer, and the two 5¼-inch flexible and hard disc drives. These were rep-

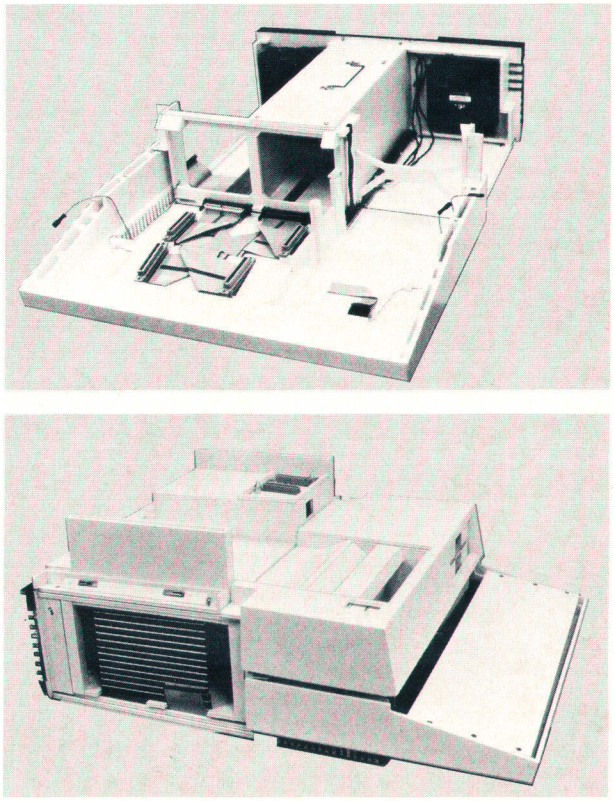


Fig. 1. *Foam-core board model of an early prototype of the package design for the HP 9000 Model 520 Computer at two assembly steps.*

resented by simple foam-core boxes while the nondefined parts took shape in models and drawings. We eventually constructed an entire machine out of these low-tech models (Fig. 1). In fact at a quarterly review, we presented a 35-mm slide show in which we sequentially showed each module or part, first by itself and then in place in the product, progressing just as production would assemble the product until we had built a finished Model 520. This gave us a high level of confidence that we understood what the various parts were, how they related and interconnected to one another, what fit, access, and airflow problems there were, etc. The only drawback was nervousness on the part of lab management because we had the design so far along, but in the wrong material—cardboard.

The foam-core board's strength as a modeling tool came from its ease of fabrication. It seems obvious that a cardboard mockup of a die casting can share little more of the physical characteristics of the real part than its shape. But it was surprising how much we could tell from the model parts—where they were weak, the real parts were weak. So they did serve to warn us of fundamental flaws in our structural design approach.

We did not go directly from foam-core board to the final tooling. Instead we took an intermediate step and created temporary tooling for most of the major parts—rubber molds and urethane parts for the structural foam components, and sand castings instead of die castings. The reasons were time and money. These temporary tools were much less expensive and the parts they made allowed us to get more quickly into the design evaluation phase because of their better structural characteristics. And when we found the need for changes, they were easy to accomplish, meaning quick and inexpensive.

Only after building several production prototypes did we start cutting hard tools. One measure of success of the design effort is the cost of the changes that had to be made to the final tooling. On at least one previous product in our division's past, we spent the tooling budget about three times. First we bought the tools, but because of the schedule pressure, the parts design had not been adequately verified and many changes were required. The total bill for tool modifications to make the changes nearly equalled the original investment. Then we started running production quantities and it became apparent that the tools were so patched up from the corrections that we needed to start from scratch and buy new tools, spending the tooling budget a third time. For the Model 520, our model-oriented design approach encouraged lots of iterations early and the use of temporary tooling to prove the design reduced the total tool bill. Of this, about 6% was spent on temporary development tools and parts, and about 9% was spent on changes to the final tools. So we didn't spend the tooling budget three times, but only 1.15 times.

So low-tech modeling paid off on both ends—early in the design phase where it enabled us to look at many alternatives and evolve the best ones quickly, and later at the end of the development cycle when design changes are so costly. All in all, our investment in modeling tools was less than $1000 (foam-core board, knives, glue guns, and glue sticks), but our savings were in the hundreds of thousands of dollars, making a nice return on our rather modest investment.

Steven R. Anderson
Industrial Designer
Fort Collins Systems Division

rear grill with aerodynamically streamlined ribs is used to eliminate high outlet pressure drop while providing structural strength and operator protection. Supplemental air inlets are provided in the sides of the base and around the top mass memory faceplate bezel to provide additional air to the processor module and the mass memory controller cards. They also compensate for any I/O chamber inlet blockage caused by the two mass memory devices.

The fans are mounted on the rear of the machine. Instead of the more common ac fans, dc fans are used. A dc fan provides more consistent air output since its supply voltage is usually regulated, while an ac fan's air output varies with a change in the ac line voltage and/or frequency. The dc fan speed in the Model 520 is increased in three discrete steps according to system load, ambient temperature, and altitude. This provides reliable system operation over a wide range of operating conditions while reducing audible noise.

Interconnect

Ideally the electrical connections to other modules and components should be completed or broken automatically when a module is inserted or removed. In the Model 520, most of the modules are designed so that this occurs. This aids in testing, and makes the final assembly of the mainframe much faster—just drop in the modules and close up the machine. But, if the automatic interconnect method is not reliable, it is not worth doing. The key problem to overcome is the alignment of the connectors. A small misalignment between two mating connectors places a lot of stress on the contacts. This usually leads to intermittent and/or hard failures. In the Model 520, alignment pins are used to locate each module accurately. These pins in the base of the machine engage receptacles in the modules to align the connectors.

Another objective was to eliminate any differential motion between mated connectors. This differential motion causes fretting corrosion on the connector contacts which could lead to connector failure. In vibration, a module can easily move slightly relative to a mating connector. Even a small movement can be detrimental. The Model 520's design uses a floating connector scheme to solve this problem. The connectors are mounted using shoulder screws so that they can move 0.5 mm in all directions. This requires a connector that can align itself with its mate without damaging any contacts even if the two connectors are initially misaligned by as much as one millimeter. Since the connector is no longer rigidly attached to the structure, it can move to eliminate all relative motion.

All this leads up to an even bigger problem—how to connect the CRT display electrically to the base. Here the problem is that the display must be able to be tilted and the connectors must locate themselves to the bottom of the display when it is set at different angles. The solution adds another level of floating alignment. The base connectors are mounted with shoulder screws to a connector plate that has two large locator pins with over 5 mm of lead-in taper per side. The plate is spring-loaded against the bottom of the CRT display to follow it through its range of motion. The connectors are as close as possible to the center of rotation to minimize their motion relative to the mainframe. When the display is installed, the locator pins find their

holes in the casting on the bottom of the display and move the connector plate to the proper position and angle. After installation, the spring-loaded connector plate follows the display as it is tilted, guaranteeing a reliable electrical connection.

CRT Display Tilt Mounting

The tilt mechanism (Fig. 3) inside each of the two pedestals supporting the CRT display performs three basic functions. It provides a spring force to counterbalance the weight of the CRT display, it has a latch to secure the display to the mainframe, and it provides adequate friction force to maintain the display in a selected position. Within the mechanical stops, the tilt is infinitely adjustable. The operator simply tilts the CRT to the position desired, and it stays where the operator leaves it. The same mechanism works for both the HP 98760A color CRT display option, which weighs over 32 kg, and the standard HP 98780A monochromatic display option, which weighs only 16 kg.

The tilt mechanism consists of five major parts: support, spring, balance arm, spring landing, and pivot. The support is the frame that holds the parts together. The spring provides the force to counteract the weight of the display. The balance arm transfers the force to the spring landing, which is mounted on the casting on the bottom of the display assembly so that it holds the balance arm at the right position to balance the display properly. The position of the spring landing is different for the two CRT display options. The pivot is also mounted to the CRT display and simply acts as a pivot point for tilting the display.

Each pedestal on the rear cover of the Model 520's base assembly provides a notch for the pivot to settle into, and then the latch simply grabs it like a finger. The display rests entirely on the pivot and spring landing as shown. The different position of the spring landing on the two different display options allows the same mechanism to counterbalance them both. No adjustments need to be made to the tilt mechanism to switch displays.

Friction is added to the system for two reasons. The counterbalance force is not exact, but an approximation. Also friction is needed to compensate for variations in spring forces, weight, center of gravity, and mechanical dimensions.

The pivot and spring landing are part of the interface module mounted on the bottom of the display. This module houses one printed circuit board and allows the color and monochromatic displays for the HP 9845 Computer to be used also on the Model 520. For future displays, the same design can be used by simply locating the spring landing in the right place.

Mechanical Design

Access to the Memory/Processor Module on one side of the Model 520 and to the I/O and mass memory card cage on the other does not allow a sidewall on the structural foam base. The resulting flat shape at the rear of the base does not have good bend resistance. Another decision caused additional concern about this inherent weakness. In the design of the keyboard area, a number of air intake openings are incorporated under a cantilevered extension of the base. This extension forms a nest for the keyboard module and provides a cable route for the electrical connections to the main printed circuit board. The air openings further weaken the base to bending. Also, the extension is subject to extra bending forces, because it is likely to be leaned upon and because it presents a convenient handle for a user wanting to move the computer.

A number of enhancements were made to the base design to provide the needed strength. The cooling air openings are reinforced by adding triangular gussets at the edge of each opening on the inside and outside of the part. The gussets also enhance the flow of plastic in the mold to fill the forward portion of the base. A reinforcement resembling an I beam turned over on its side is incorporated into each base sidewall. The most important structural addition is attached to the planar rear part of the base: another I-beam structure was added lying down and fastened to the base (Fig. 2b). A die-cast aluminum rear panel forms the top of the I and another die casting forms the bottom of the I. A folded aluminum sheet-metal part with a U-shaped cross section joins the two castings. The module adapter plates or covers tie the forward and rear castings together for added strength. An extruded aluminum strip is screwed to the front and rear castings on each side to further support the base. This extrusion can be removed to service the CPU and mass memory boards. Two rubber rollers are installed at the rear of the base to aid in moving the Model 520, because the combined weight of the color CRT display option and the mainframe can be as much as 73 kg. The computer can be raised by using the cantilevered keyboard as a handle to clear the front footpads from the resting surface and then it can be wheeled to a new position.

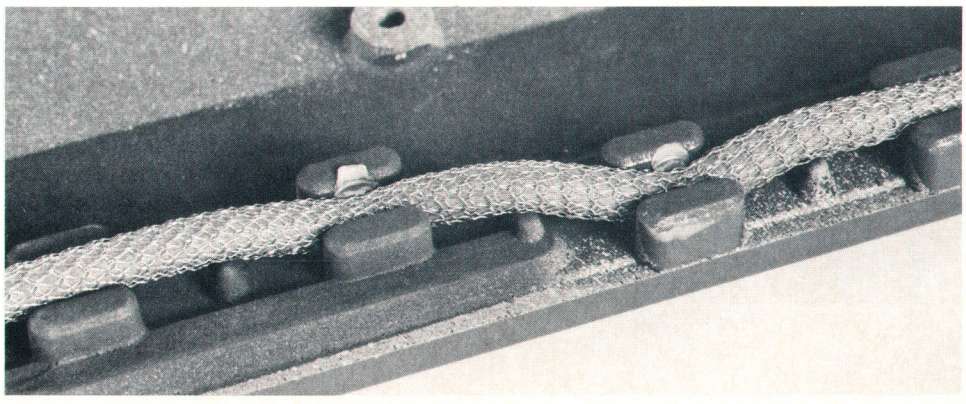


Fig. 4. *The conductive rope gasket used to seal the Model 520's enclosure against EMI is located between the case halves and retained in place by ultrasonically deforming two parallel rows of oval bosses as shown. The triangular ramps ensure conductive contact between the case halves.*

The design was modeled using 6-mm thick plywood for the base and folded 2.5-mm thick aluminum for the castings. A goal of less than 3 mm of deflection at the joint between the mainframe and the keyboard was set so that there would be a safety factor to prevent excessive flexural relative movement between electrical connector pairs. Such movement can cause disengagement or fretting of the metal contact surfaces of the connectors and lead to failure. The initial model demonstrated a deflection in excess of 3 mm between the base sidewall and the front casting. The joint is made acceptable by adding a 2-mm thick piece of aluminum bent into an L shape in two directions to provide stiffness. This piece is screwed to the sidewall and bolted to the casting. The folded sheet-metal model simulated the casting successfully. Sheet metal could have been used in production in place of the castings for structural reasons, but die casting offers versatility for fastening modules, making contact with conductive EMI gaskets, and mounting fans, and it provides adequate strength with less material and fewer process steps. The plywood model was duplicated several times and used to support the monochromatic or color CRT displays and the prototype keyboard assembly. These units were used for hardware and software testing of breadboard electronics and the prototype stage of the Model 520.

Electromagnetic Compatibility

Suppression of electromagnetic interference to meet regulatory agency limits is accomplished by spraying the interior of the structural foam plastic parts with a conductive nickel-base paint. A cylindrical woven wire mesh with a compressible foam-rubber core rope is attached to the interior of the housing parts. This material compresses against the metal-encased modules at their outside interface with the base and covers, forming a seal around the periphery of the mainframe to prevent electromagnetic waves from getting in or out. Tradeoffs between EMI sealing and cooling air flow requirements are made at air inlet and outlet areas. Wire screen is placed over the air inlet openings in contact with the conductive coating on the inside of the base and an open grid pattern is cast into the rear-panel air outlets to satisfy both requirements.

The optimum compressive force for the selected gasket material is 0.67 kg/cm. Since the periphery of the mainframe is approximately 2540 cm, we faced another distortion problem when the covers were attached. The covers were pushed away from the mainframe in areas away from the captive fastener locations. The problem is overcome by incorporating a channel to retain the gasket rope and provide intermittent contact. The channel is established by a double row of oval bosses raised off the interior of the structural foam part (Fig. 4). The intermittent contact is provided by placing a triangular ramp midway between each pair of oval bosses. A 30-mm interval between ramps provides enough contact pressure to suppress emission of EMI from the housings and to reduce the compressive forces between covers and modules by 75%. The gasket rope is retained in the channel by an ultrasonic staking process on selected boss pairs. The cut ends of the rope are potted with a silicone rubber and terminated within the structural foam housing in holes molded into bosses at the ends of the channel.

Fasteners

The quantity of screw fasteners can become large in a computer of this size. Different lengths and sizes compound the problem of putting the correct screw in the correct place. A goal to minimize the number of different kinds and sizes was set. There are five types: captive screws for the housing covers, captive screws of another type for the modules, self-tapping (into plastic) screws, and two machine screws (metric 3 and metric 3.5). The total quantity of fasteners is minimized by using as large a screw as possible for each application. The larger screws meet strength requirements with fewer numbers. The decrease in assembly time by having fewer fasteners is enhanced by the use of air-powered, adjustable-torque drivers on the assembly line.

The captive screw assembly in the covers is based on a regular M4 pan-head machine screw. A flat washer and an external-tooth locking washer are installed under the screw head and the screw is then installed into a metal insert that is ultrasonically pressed into the cover. The screw is retained in place by pushing a neoprene rubber O ring over the screw threads. The holes in the cover for the captive screws are oversized to provide for alignment tolerances. In the original design of the cover this left too small an area in contact between the washer and the hole. Hence, the screw tightening torque of 1.4 N-m caused compressive failure of the plastic. The metal insert mentioned above is required to overcome the compressive load of the screw head.

The captive screw used for the modules is a swaged-on spring-loaded commercial assembly. The spring loading is necessary to keep the threads from interfering when seating the module on its connector. The swaged-on design and the addition of a washer allow movement of the assembly to align the screw to its mating threaded socket in the base assembly.

The self-tapping screws used to fasten structural components to the plastic base have a special head. The tolerance analysis for fastening showed that a washer would be required to transfer the tightening torque safely. The hole size for the fastener determined by the analysis does not leave enough bearing area between the part to be fastened and a common screw head without the addition of a washer. A standard hex-washer screw head style has sufficient area, but requires a different drive. A common drive is desirable on an assembly line using air-powered drivers. By combining the common drive recess with the hex-washer head style, it was possible to retain a common drive and eliminate the separate washer necessary for use of other head styles.

Acknowledgments

Many thanks to everyone who became involved in the plastic processing department. Special thanks to Walt Heron for his ultrasonic staking idea, to Bill Toben for his work on the conductive paint, to Sandy Degi for her help with all the plastic parts, and to the molding department for their efforts in tool tryouts. Linda Johnson, Bev Hemstreet, and Gretchen Honick spent many hours helping

(continued on page 11)

The Toleranced Design of the Model 520 Computer

Some attention to the effects of dimensional variations in component parts is a normal part of the design of any assembled product. In the case of a product as densely packed as the HP 9000 Model 520 Computer, this attention is particularly critical, requiring a painstaking consideration of the accumulated effects of individual tolerances to ensure easy assembly of the product and easy replacement of any failed modules later in the field.

To review some basic principles, a tolerance is the allowable range of variation in the dimensions of a part. These tolerances may be unilateral or bilateral. A unilateral tolerance is taken to one side of a dimension (e.g., a hole diameter of 3.0 +0.13 mm). A bilateral tolerance occurs on both sides of a dimension (e.g., a hole position of 10.0 ±0.13 mm).

Tolerances have a variety of origins. As the equipment for forming sheet-metal parts wears, lead-screw backlashes increase, as do punch-to-die clearances. These effects produce variations in hole placement and diameter. When a plastic part is molded, it is subject to inconsistent shrink rates and constituent material variations. The final part produced has dimensional changes as a result. In any kind of molding or casting operation the cooling of the molten material to the solid phase results in internal stresses, thus warping the parts produced.

If tolerances are not accounted for in the design of mechanical parts, several problems arise. The predominant problem is difficult or impossible fits during assembly. As these fit problems are discovered on the production line, redesign for tolerances must occur to correct them. These corrections take place through part specification revisions, obsoleting parts in stock, documentation updates, etc. In some instances, it may not be possible to solve a tolerance problem, forcing production problems to continue for the entire product life cycle. Some tolerance problems result in long-term intermittent electrical connections, requiring repetitive servicing of equipment that only works after merely taking it apart and putting it back together again.

The benefits of a toleranced mechanical design are many: easier production line assembly, minimal production changes, increased electrical interconnect reliability, and generally, a better product. The ability to use parts manufactured with tolerance errors is increased. This allows the production line to continue manufacturing where otherwise it would be halted.

A worst-case tolerance T_i is typically assumed to be three times the standard deviation in the Gaussian distribution of the errors in the actual length of a dimension. If a dimension is specified as 1 ±0.1, this means that its mean value is 1 with a standard deviation of 0.1 divided by 3, or 0.033. Thus, a dimension greater than 1.1 or less than 0.9 will occur at a frequency of 0.27%.

The overall standard deviation is the square root of the sum of the squares of the individual standard deviations, or

$$\sigma_\Sigma = \sqrt{\Sigma\sigma_i^2} \qquad (1)$$

Since the typical bilateral tolerance is three times the standard deviation for a dimension, this equation may be restated as

$$T_\Sigma = \sqrt{\Sigma T_i^2} \qquad (2)$$

This equation can be used for the sizing of a screw clearance hole. For example, assume that a printed circuit board and a sheet-metal plate are in perfect relative position, with zero location error between them (Fig. 1a). These two parts need to have a screw attaching them. The screw protrudes through the printed circuit board and attaches to a hardware insert pressed into the sheet-metal plate. To analyze what the screw hole clearance must be, the following tolerances must be known:

Dimension	Tolerance
Sheet-metal hole position	0.13 mm
Sheet-metal hole clearance	0.02 mm
Insert outside diameter	0.025 mm
Insert screw thread concentricity	0.02 mm
Printed circuit board hole location	0.13 mm
Printed circuit board hole diameter	0.06 mm

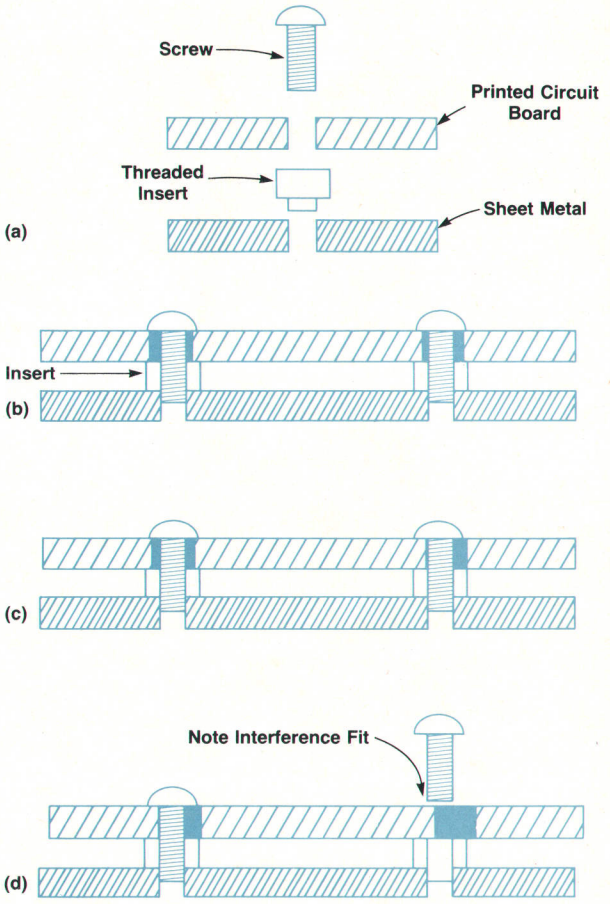


Fig. 1. *Printed circuit board clearance hole sizing. (a) Single mounting screw to attach board to sheet-metal plate. The size of the hole in the board for the screw must be large enough to accommodate some misalignment and variation in part dimensions. (b) Printed circuit board in perfect position relative to the sheet-metal plate. Note the misaligned holes in the board for the two mounting screws. (c) Board skewed relative to plate, but the hole dimensions still allow the mounting screws to fit. (d) The mounting screw on the right does not fit because the screw on the left was tightened prematurely with the board extremely skewed relative to the plate.*

To determine the screw clearance hole dimension, the overall tolerance is determined from equation (2):

Tolerance		Square of Tolerance
0.13		0.0169
0.02		0.0004
0.025		0.000625
0.02		0.0004
0.13		0.0169
0.06		0.0036
sum: 0.385*	sum:	0.038825

Square root of sum of squared tolerances: 0.197*

The result is the bilateral tolerance that should be allowed for the radius of the clearance hole.

When the printed circuit board and the sheet-metal plate are in perfect relative position, the above clearance hole will work with a 0.27% rejection level. To ensure perfect relative position, all of the screws fastening the board to the plate must have been started, but not tightened, as indicated in Fig. 1b. This guarantees that the two parts are either in perfect relative position, or at least close enough to be functional as an assembly as depicted in Fig. 1c. If one screw is tightened before the other screws are started and the board is skewed too much relative to the plate, the other screws will be impossible to fasten as shown in Fig. 1d. In this case, the tightened screw(s) can be loosened to allow the relative position to shift for successful assembly.

This screw attachment example illustrates an extremely common and simple problem. It also demonstrates how to use the statistical tolerance method. While this example may not seem very important, some worst-case clearances in practical product design situations can exceed the screw head diameter, requiring a washer to allow proper tightening of the screw. The very same situation, when analyzed statistically to select the correct dimensions, may not require any special treatment.

On the Model 520, our final design resulted in a three-level approach. The three levels are attached to each other at controlled interfaces, enabling the control of tolerance accumulations. These three levels of attachment take place at roughly the front-to-back and side-to-side midlines of the Model 520's base. This allows tolerance accumulations to be more evenly distributed about the instrument from a location near its central vertical axis.

The base is the first level and provides locating features for the structural casting assembly, which is the second level. The keyboard electronics, keyboard bezel, disc drives, and front cover are directly located by the base. This ensures close positioning to the base, and using only one major interface allows few tolerance accumulations.

The structural casting assembly is the second level of the toleranced design. It is composed of a front casting, a right-front casting, a power supply housing, and a rear casting. The casting assembly is located relative to the base by means of a locating pin pressed into the base and projecting through a tight clearance hole in the front of the casting assembly. To locate the casting assembly along the centerline of the base, two tapered indentations in the bottom of the rear casting fit over two pedestals with tapered sides cast in the rear of the base (see Fig. 2b on page 4). The tapered fit of the base relative to the rear casting allows for a considerable variation in differential lengths from front to back, while providing negligible variation in lateral positioning.

The positioning of the I/O backplane against the power supply housing locates the mainframe motherboard. As the casting assembly is installed in the base, the motherboard/backplane assembly is formed. The final attachment of the casting assembly to the base then sandwiches the motherboard into its permanent location. Thus, no fasteners are required to hold the motherboard in place. After the motherboard is installed, the power supply and Memory/Processor Module can be installed.

The mounting plate of the processor module is located by a closely positioned hole-insert pair at the top center of the front casting. Rotational alignment is accomplished by tapered pedestals in the rear casting in the same manner that the structural casting assembly is located with respect to the base. The I/O area is similarly attached to the top of the right-front casting. The processor mounting lid floats relative to the processor module, allowing simultaneous stress-free electrical interconnect of the processor module and accurate positioning of the mounting lid.

Both the processor mounting lid and the I/O lid planes have inserts projecting vertically to align the position of the rear cover. The positioning method used is similar to that used in the base-to-casting assembly: one point locates the cover in two dimensions, another references the angle.

The integral printer is hung from the front casting, with its position set by base aligning pins.

It was determined that the most critical part in the overall toleranced design is the structural casting assembly. In this assembly, the power supply module housing was found to be the most critical part, and was tooled as a class-A stamped and formed part. In addition, the holes in the casting are drilled using drill jigs with tight tolerances.

Joseph R. Milner
Product Designer
Fort Collins Systems Division

*Note that the worst-case tolerance is 95% worse than the statistical tolerance (0.385 compared to 0.197).

us make the Model 520 manufacturable.

Brad Clements was a remarkably dynamic and effective materials engineer. Thanks also to Cliff DeLude who did the original conceptual design and to Priscilla Berwick for her help with drafting.

References

1. J.M. Mikkelson, et al, "NMOS-III Process Technology," *Hewlett-Packard Journal*, Vol. 34, no. 8, August 1983.
2. J.W. Beyers, E.R. Zeller, and S.D. Seccombe, "VLSI Technology Packs 32-Bit Computer System into a Small Package," *ibid.*
3. D.D. Georg, B.D. Osecky, and S.D. Scheid, "A General-Purpose Operating System Kernel for a 32-Bit Computer System," *Hewlett-Packard Journal*, Vol. 35, no. 3, March 1984.
4. S.W.Y. Wang and J.B. Lindberg, "HP-UX: Implementation of UNIX on the HP 9000 Series 500 Computer System," *ibid.*
5. D.M. Landers, et al, "An Interactive Run-Time Compiler for Enhanced BASIC Language Performance," *ibid.*

Color Graphics Display for an Engineering Workstation

by Daniel G. Schmidt

MANY PEOPLE THROUGHOUT HISTORY have emphasized the importance of visual images in human communication. The computer, being nonhuman, prefers numeric or, at best, alphanumeric communications. This conflict is the father of the color graphics subsystems for computers. With such a subsystem, a computer can deliver information to users in a much more efficient way. The proper use of color graphics can aid in simplifying the interpretation of large amounts of complex data.

Cost is a major concern when considering the addition of color graphics to a computer system. The cost of an item must be weighed against its perceived value before a decision can be made as to whether the item is worth the price. If color graphics can be supplied at a lower cost, then its advantages can be made available to more users.

The HP 98760A Monitor Assembly is a color graphics display subsystem designed for the HP 9000 Model 520 Computer with these goals in mind. The 98760A can display both alphanumeric (alpha) and graphics information on its 13-inch-diagonal color CRT using a raster-scan format. The alpha and graphics rasters are separate and can be displayed individually or together. The system software supports new features such as color map graphics and raster size, and emulates displays of earlier systems such as the HP 9845C Computer.[1]

Graphics Attributes

The graphics raster fills the entire screen and is 512 pixels wide by 390 pixels high. The horizontal size of a graphics pixel is 1.5 times that of an alpha pixel. Hence, the alpha raster is narrower than the graphics raster by 32 graphics pixels and is centered within the graphics raster (Fig. 1).

Four memory planes are available for the graphics raster with each pixel individually addressable. (The alpha display is not color mapped; alpha colors are handled differently as will be explained later.) The graphics memory planes address a color map that can generate up to 16 colors per frame. That is, the video circuitry is capable of displaying any choice of 4096 colors by altering the voltage on each of the three CRT guns (16 levels per gun), and the color map can contain references for 16 choices. This allows the user to display single pixels of any of the selected 16 colors at the same time at different locations on the screen. The system software also uses the pixel dither patterns[2] used in earlier HP eight-color displays to provide a variety of eye-averaged colors that can be used at the same time as the color map to provide area fill and shading. This allows display of up to 4913 eye-averaged colors using only 8 of the 16 color map locations. This is simply emulating HP's earlier eight-color displays by devoting half of the color map to the basic eight colors. This gives the 98760A a great degree of flexibility and backward compatibility with earlier HP color displays.

The graphics circuitry uses a UPD7220 graphics display controller IC, which is an intelligent graphics peripheral controller. This controller has at its disposal 64K×16 bits of dynamic graphics RAM. This RAM contains color map information for each of the graphics pixels on the screen, and can be accessed by the Model 520 via the graphics controller. Using a graphics controller simplifies the circuitry and reduces the cost of the display without a great loss in performance. This graphics controller generates vectors for the 98760A at a speed greater than 28,000 pixels per second.

Alpha Attributes

The alpha raster is 720 dots wide by 390 dots high. Alphanumeric characters are 9 dots wide by 15 dots high and the alpha raster can display 26 lines of 80 characters each. The character set includes the 128 ASCII characters, a semigraphic line drawing set, and either the HP European extension or the Japanese Katakana characters. The local language extensions are detailed and are comparable to those used in other HP products.

The alpha display and many of the sync signals used by the analog circuitry are controlled by an MC6845 CRT controller IC located on the circuit board in the casting underneath the CRT. The MC6845 requires system software initialization to provide the proper sync signals for either 60-Hz or 50-Hz operation.

The attributes for the alpha characters are contained in six signals: UL (underline), IV (inverse video), BL (blinking),

(continued on page 14)

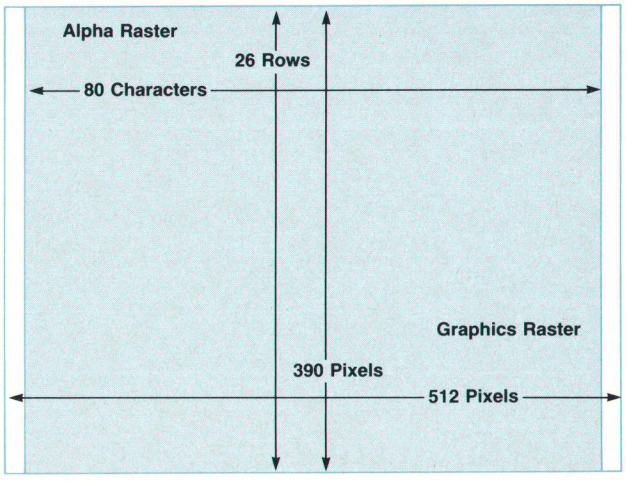


Fig. 1. *The graphics raster for the HP 98760A Color Display fills the entire screen. The alpha raster is slightly smaller horizontally and is centered on the graphics raster as shown.*

Detached Keyboard Option for the Model 520 Computer

Late in the design phase of the HP 9000 Model 520 Computer, after most of the parts were already tooled, the German ergonomic standards ZH1/618 were first proposed.[1] The Model 520 was designed as an integrated workstation and like other HP desktop computers has many features packaged together—two mass memory devices, a printer, a power supply, a Memory/Processor Module, a CRT display, an I/O card cage, and a keyboard. When the initial product design was compared to the proposed ergonomic standards, some discrepancies were noted. Some were easily brought into compliance, such as going from dark keycaps to lightly colored, textured keycaps. To achieve proper working heights for the keyboard and CRT, a special table was designed and is available through HP's Computer Supplies Operation. The biggest noncompliance with the ergonomic standards was that the Model 520's keyboard was fixed with respect to the display. The only adjustment available between the keyboard and display was a self-holding tilt feature for the CRT. Detaching the keyboard from the display was not possible. A follow-on design project was initiated to correct that deficiency.

There are a few different ways to detach the keyboard from the display. One obvious method is to package the keyboard separately and mold a new base for the rest of the machine. Similarly, detaching the CRT from the base would be a way to meet the standard. These two solutions were undesirable because of high tooling costs and difficult cabling. Also, neither solution is easily interchangeable with the existing design. For manufacturing simplicity and possible modification by customers, the use of parts already used in the standard machine is best. The detached keyboard was also needed quickly since the proposed ergonomic standards were scheduled to become mandatory in Germany. The best solution would be quick, use most of the same parts, and minimize tooling and development costs.

The Model 520 keyboard consists of a purchased keyboard assembly and an HP-built scanner board. The scanner board interfaces with the rest of the machine through the I/O processor bus and receives and distributes the power for the keyboard. The keyswitch assembly and the scanner board are electrically connected with a 20-line flat cable. The major challenge of the detached keyboard design for the Model 520 was determining what to do with the scanner board. If placed outside the machine, up to 100 signals would have to go with it. The cable would be very large and require very good EMI shielding. If it stayed in a shortened base, the only volume available for the board was either across the front of the machine, which would block cooling airflow, or standing next to the printer as a two-board package. A two-board package would have required much more development time and a new place to mount the Model 520's beeper. The easiest solution was to leave the base and scanner board assembly intact and just bring out the 20 signals between the scanner board and the keyswitch assembly. That was the method chosen. The result is shown in Fig. 1.

Leaving the scanner board in the base required covering the board and providing for its mechanical mounting. In addition, the cover and mount must make all of the necessary conductive connections to the RFI gaskets, and provide a place to mount an interconnect/buffer printed circuit board. Those functions are carried out by a welded sheet-metal assembly. A molded cover snaps onto this piece and provides a surface for the keyswitch assembly to rest on. A removable extension is provided to give more surface for the keyboard. The extension can be stored under the molded cover along with flexible discs, tapes, and other thin items.

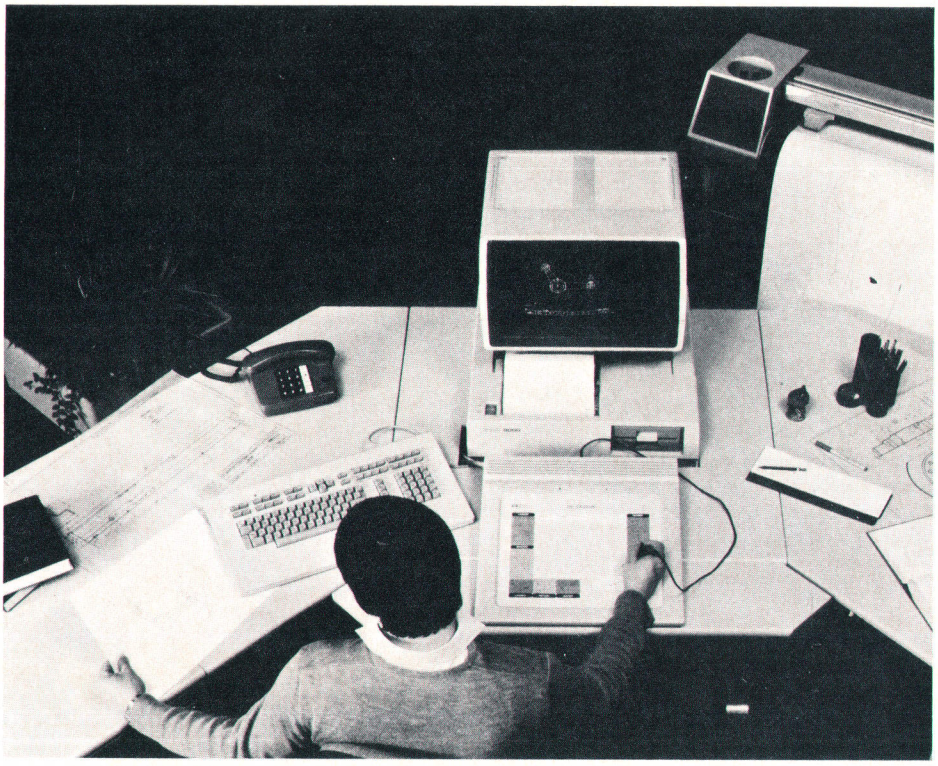


Fig. 1. *The detached keyboard (Option G02) of the HP 9000 Model 520 Computer is available in Europe and complies with German ergonomic requirements specified by the ZH1/618 standard.*

The keyswitch assembly is packaged between a sheet-metal base and a structural foam molded bezel. The cable connection to the mainframe is made at the keyboard and is fully hidden under the rear overhang of the bezel. The rear overhang also provides a recess for the cable. When the keyboard is placed on a table, it can be tilted to a 10-degree angle using its built-in folding legs.

The keyboard cable is 90 cm long, providing enough cable to place the keyboard to the right or left of the base, or on the operator's lap. The cable tucks into the recess in the back of the keyboard and drops into a hole at the back of the base cover. The final solution meets the German ergonomic requirements, ZH1/618. The option is easy to add at any time and requires less than 20 special parts. The major drawbacks of this solution are that the keycaps are higher than those of the fixed keyboard when the detached keyboard is sitting on the scanner board cover and that the front end of the computer sometimes gets in the way. To solve these problems, another work table was designed that has a recessed area for the main computer and a movable work surface that can cover the front of the machine. The work table also makes it possible to place a graphics tablet directly in front of the CRT display with the keyboard located to either side.

The detached keyboard version, Option G02, of the Model 520 and its companion work table are available only in Europe at this time.

Reference

1. P. Arnold, "Ergonomics with bite: New video display standards," *Electronic Business*, Vol. 10, no. 2, February 1984, pp. 222-223.

Michael K. Bowen
Product Designer
Fort Collins Systems Division

R (red), G (green), and B (blue). Each 9×15 character cell can be individually addressed with respect to each of these attributes. This allows each character in any combination of characters to be one of eight different colors: red, green, blue, yellow, cyan, magenta, white, and black. And, each character in any combination of characters can be underlined and/or blinking and/or inverse video. These attributes are the same in the 98770A High-Performance Color Display so that user programs will run on both displays.

Alpha pixels are dominant over graphics pixels. Whenever an alpha pixel is present, it is displayed undisturbed, while a graphics pixel at the same location on the screen is not visible. Because aesthetic concerns required the widening of just the inverse characters to make them more visible, a circuit to stretch the rising edge of each inverted alpha pixel by one half is included in the 98760A. If the character is not inverted, the stretch circuit is turned off.

Hardware Design

A block diagram of the color graphics circuitry is shown in Fig. 2. The video shift registers consist of three 16-bit latches and four 16-bit shift registers. To reduce the cost, these shift registers are incorporated into an output gate array. The gate array receives data bits in parallel from the graphics memory for display refresh and shifts these bits out, four at a time, at the graphics video rate.

The gate array design lowered the cost and raised the reliability of the system by eliminating many TTL packages. The estimated failure rate of the one chip compared to its TTL equivalent shows a marked improvement in reliability. The cost savings came mostly in the board space saved. Without the gate array, the digital board could not have contained all of the necessary TTL logic. Since the board size was fixed by its location in the mechanical layout, a design to accommodate a larger board would have been much more expensive.

The outputs of the color map RAM define the colors seen on the face of the screen. The color map RAM consists of three high-speed 16×4-bit static RAMs which map a four-bit address into 12 bits of color information. The graphics RAM contains an address to the color map for each graphics pixel. Each four-bit field from the color map is used to drive a different gun in the CRT to one of 16 levels of intensity. The addresses applied to the RAM come from a multiplexer, which can select either the four video lines from the graphics shift registers (output gate array) for display refresh or the DB12 to DB15 data lines from the Model 520's I/O processor bus to allow the Model 520's CPU to access the RAMs.

The video mixing circuitry mixes the alpha video with the graphics video, making alpha dominant over graphics. Advanced Schottky TTL circuits are used for the digital-to-analog (D-to-A) drivers to obtain fast rise and fall times, and to reduce skew between the red, green, and blue color channels and the high-to-low and low-to-high transitions. The graphics lines are fed into five NAND gates in each channel with the combined blanking signal able to gate the graphics off. A sixth NAND gate in each channel is devoted to alpha and is driven only when the graphics display is forced off by the alpha pipeline. The single alpha driver is

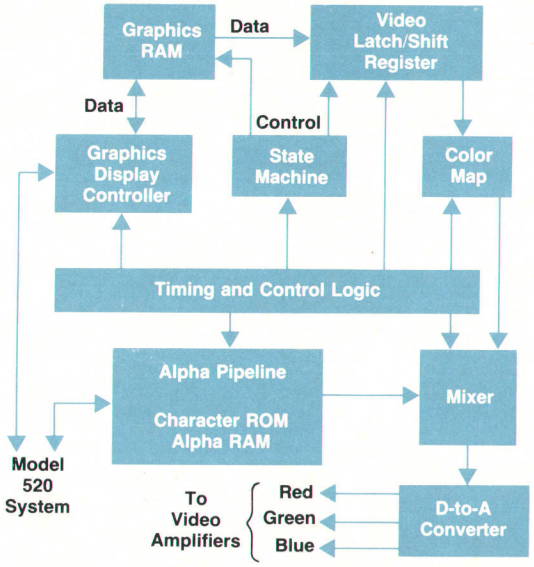


Fig. 2. *Block diagram of color graphics circuitry for the 98760A.*

made equivalent in CRT brightness to all five graphics drivers combined by using a smaller D-to-A resistor value.

The D-to-A and bias voltage circuits provide the interface between the digital video signals and the analog drive requirements of the video amplifier input stage. The interface signal yields increasing display brightness with increasing sink current. The beam-off level corresponds to black on the display. Because of the variations and drift of the cutoff voltages for each gun in the tube, it is necessary to make the change in sink current between black and the first visible shade larger than the step size between adjacent visible shades. The threshold of visibility is set approximately halfway between black and the first visible shade. This guarantees that the black level will always yield black on the display and that the lowest shade will be visible. The remaining steps between shades are equal in size.

The D-to-A circuit was chosen for its cost/performance ratio. The D-to-A circuit is fast and is coupled directly to the video amplifier, which has a 12-ns rise time. Current is sunk through the resistors in an 8-4-2-1 weighted resistor network. A fifth resistor receives an offset signal, which is present whenever a nonblack graphics dot is being displayed. This causes the larger sink current step between the black level and other brightness shades.

All components and component values in the 98760A are critical for proper operation and suppression of EMI (electromagnetic interference). Changing the individual boards in the system could result in poor picture quality because of variations in the exact values of the components on the boards. To reduce repair costs and avoid the need to readjust the CRT when a board must be replaced, a means was devised to add a special resistor on each board at the factory that compensates for measured differences in the component values.

The 98760A Color Display meets the requirements for EMI suppression, level B. This was difficult to achieve because of the fast (51-MHz) video circuitry, but it qualifies the device for unlicensed residential use.

Cost

The 98760A has a low price for four main reasons. The output gate array and the discrete D-to-A converters have already been mentioned. Another reason was the leveraging of the printed circuit and tube assemblies used for the color display of the earlier HP 9000 Model 236 Computer (formerly designated as the HP 9836C). The video board, sweep board, power supply, and CRT tube are used in both the Model 236's color display and the 98760A (Fig. 3). This reduced the R&D investment and lowers the production costs of both systems.

The fourth reason for lower cost is the use of an in-line CRT tube. Although the color purity is not as good as that attainable with a delta-gun configuration, it is acceptable and using in-line tubes lowers the cost considerably. The CRT's yoke is matched to the tube, which eliminates both drift and the need for user convergence. Built-in convergence and purity simplifies the vertical and horizontal sweep circuits so much that while providing adequate performance in noncritical applications, it also produces a more efficient and reliable product at a greatly reduced cost.

Acknowledgments

Recognition should be given to the entire design team headed by Bill Hale. Darel Emmot and Roger Swanson worked on the gate array and Dave Lungren and Joe Milner did the mechanical design. Bob Fredrickson worked on the graphics processor and system testing as well as the gate array. Kathy Osborne, Mary Sue Rowan, and Mitch Stein wrote the software handlers for the product. Tom Bartz worked on product definition and Leonard Lindstone worked closely with us on the EMI testing and qualification. Also special thanks to the Model 236 Computer's color display design team for their support of the assemblies that are shared by the 98760A and the Model 236.

References

1. *Hewlett-Packard Journal*, Vol. 31, no. 12, December 1980.
2. H.L. Baeverstad, Jr. and C.C. Bruderer, "Display System Designed for Color Graphics," *ibid*, p. 29-31.

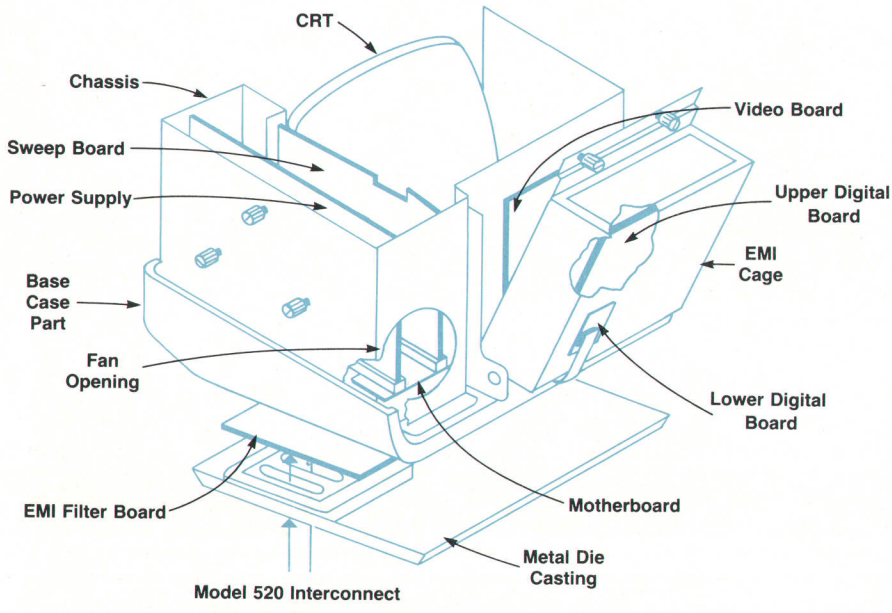


Fig. 3. *By using the same assemblies for portions of different HP display options, the manufacturing cost can be reduced considerably. The assemblies indicated are used by the color display options for both the Model 236 and the Model 520 Computers.*

BASIC Language Graphics Subsystem for a 32-Bit Workstation

by Kenneth W. Lewis, Alan D. Ward, and Xuan Bui

THE GRAPHICS LANGUAGE SUBSYSTEM for the HP 9000 Model 520 Computer provides high-performance, device-independent, interactive graphics via BASIC language keywords. The rich set of features and the friendly BASIC environment facilitate construction of such applications as data display, graphical monitoring of real-time events, two- and three-dimensional drafting systems, and CAD modeling systems.

Two major objectives guided the definition of the graphics subsystem—increase the performance and extend the power and functionality of the graphics language used in the earlier HP 9845C Computer.[1,2] The graphics language extensions were influenced by the ACM SIGGRAPH CORE standard. The interest in this standard was caused by a growing number of implementations and users in the industry. The AGP graphics package for the HP 1000 Computer and the Series 500 HP-UX operating system is based on this standard as a precedent. Therefore, the graphics extensions made for the Model 520 are functionally similar to those defined by CORE. Transportability of existing HP 9845C programs is an important consideration for current customers upgrading to the Model 520 Computer. This provided the objective to generate a product that is a superset of the language used in the HP 9845C.

Graphics Features

Multiple Device Access. The HP 9845C introduced the concept of multiple plotting devices. This concept was extended to include the logical view surface concept defined by the CORE standard. Also, multiple active input devices are now available with this new system. The selection of graphics devices is done dynamically during the execution of a BASIC program.

2-D and 3-D Plotting. Both two-dimensional and three-dimensional line and surface primitives are provided. Lines can be specified by individual BASIC statements, or an array of lines can be constructed and plotted with one statement. Regular and irregular polygons can be generated and filled with the desired color. Two-dimensional and three-dimensional modeling and viewing transformations are provided for generating an image from these primitives (Figs. 1, 2, and 3). The specification of these transformations uses the same model as the AGP graphics package, facilitating a common understanding of both packages and transportation of programs. The transformations can be used for generating instances of objects and nesting of subobjects, as well as for positioning a view of these objects.

Three-dimensional viewing transformations are highly intensive in floating-point operations. The Series 500 CPU

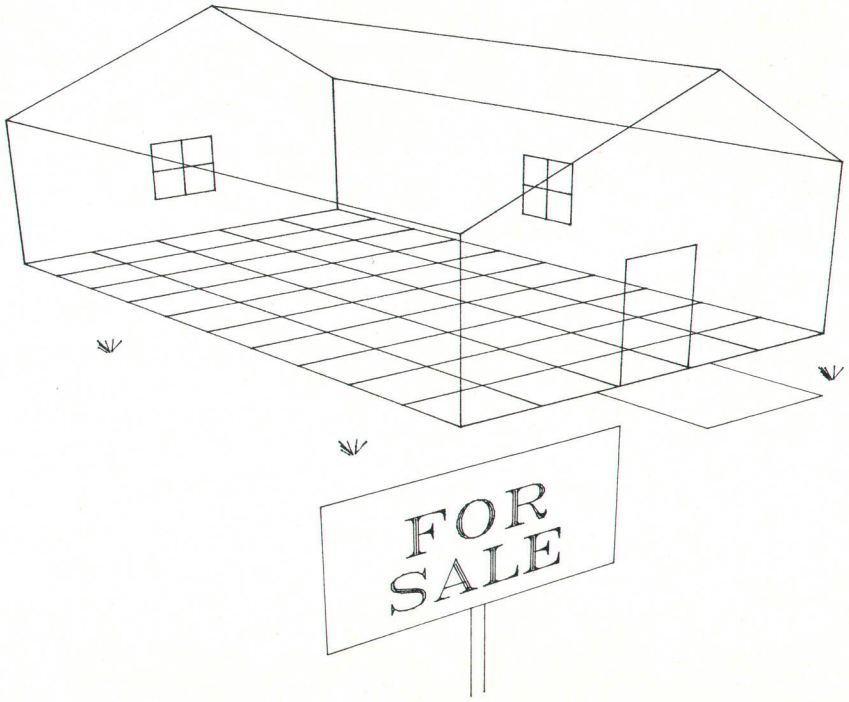


Fig. 1. *Three-dimensional view generated by the Model 520 BASIC graphics subsystem. A portion of the program for this view is given in Fig. 2. Note that text can be treated as a graphics object (For Sale sign).*

```
 10 GINIT 3D                          ! INITIALIZE GRAPHICS SYSTEM TO 3D
 20 VIEW POINT 12,4,-45               ! SETS THE POINT YOU ARE LOOKING AT
 30 VIEW NORMAL 18,-10,-30            ! SETS THE DIRECTION YOU ARE LOOKING
 40 WINDOW -1,1,-1,1                  ! SETS WINDOW TO BE CENTERED ABOUT VIEWPOINT
 50 VIEW DISTANCE 70                  ! SETS DISTANCE FROM VIEWPOINT TO WINDOW
 60 PROJECT PERSPECTIVE 0,0,-2        ! ESTABLISHES A PERSPECTIVE VIEW: I.E.,
 70                                   ! DEFINES A VIEWING PYRAMID ALONG WITH WINDOW
 80 PLOTTER IS "INTERNAL"             ! INITIALIZE PLOTTER
 90 GRAPHICS ON                       ! TURN GRAPHICS RASTER ON
100      CALL Draw_sign
110      CALL Draw_house
120      CALL Draw_grass
130 END
140 !
160 SUB Draw_sign
170 ! This subroutine draws a For Sale sign
180      PEN 1
190      MOVE 8.1,3.5,-15
200      GTEXT ORIENT -1,0,0,0,1,0   ! SETS GRAPHICAL TEXT ORIENTATION
210      GTEXT SIZE 1.1,1.0          ! SETS SIZE OF GRAPHICAL TEXT
220      GTEXT JUST .5,.5            ! CENTER-JUSTIFIES THE GRAPHICAL TEXT
230      GTEXT "FOR SALE"
240      MOVE -4,0,-20               ! THE FOLLOWING SEQUENCE DRAWS THE
250      DRAW -4,2,-20               !      SIGN AROUND THE TEXT
260      MOVE -4.2,0,-20
         •
         •
330 SUBEND
340 !
350 SUB Draw_house
360 ! This subroutine draws a house
370      MOVE 0,0,-30
380      DRAW 0,0,-45
         •
         •
600 SUBEND
610 SUB Draw_grass
         •
```

Fig. 2. *Partial listing of graphics program for view shown in Fig. 1. See Fig. 3 for a depiction of the viewing parameters specified in lines 20 to 60.*

provides high-performance floating-point operations for these transformations.[3] The hardware is an excellent match for the 3-D features.

Graphical Text. The AGP and CORE definitions provide mechanisms for including text as part of objects within a picture. The text can be positioned, scaled, and rotated to be part of a 2-D or 3-D object. For example, a viewed scene might include a sign with text on it (Fig. 1). The text and the other primitives composing the object are displayed as specified by the current viewing transformation. By comparison, graphics labels in the HP 9845C are not part of the object, but are used to annotate a plot. Changing the view of the object changes the position of a label, but not its appearance. These labels act as if they were overlays on the view surface. Thus, the label remains legible independently of the view of the object selected.

Both of these types of graphical text are useful depending on the job to be done. Model 520 BASIC provides statements to generate both types. In addition, the fonts used for generation of the characters can be defined by the user. Thus, Gothic or Roman characters can be viewed as part of an object or used to annotate a plot.

Input Device Tracking. Interactive graphics systems use input device tracking to provide operator feedback. The position of a locator graphics input device is echoed on a plotting device. For example, the position of the stylus on an HP 9111A Graphics Tablet is mimicked on the integral display of the Model 520 by using the graphics cursor of the display. The Model 520 BASIC graphics system allows this tracking to be done concurrently with the execution of the user's program. This is implemented via a tracking process that executes asynchronously with the process executing the program. Thirty times a second the tracking process wakes up, reads the locator device position, updates the plotter echo position, and goes back to sleep. This provides a smooth, continuous updating of the echo position, facilitating operator interaction with the program. In turn, the program does not need to be concerned with continually providing the operator with this feedback. Tracking can, of course, be terminated, or it can be established

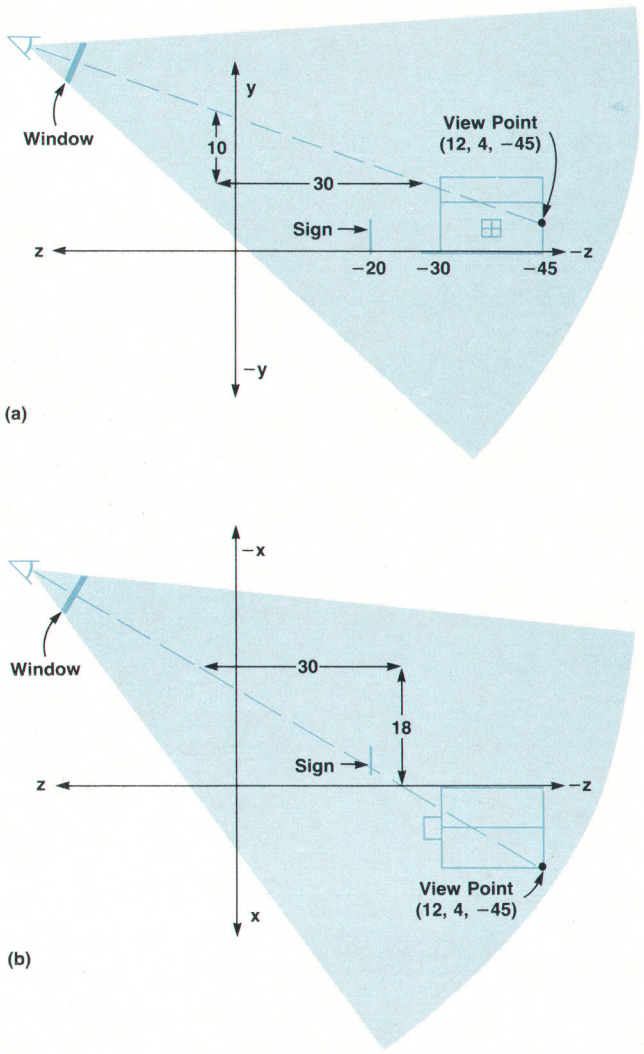


Fig. 3. *Viewing pyramid (shaded area) specified by program given in Fig. 2 as seen (a) looking along Y axis from +y to −y, and (b) looking along X axis from +x to −x. The coordinates of the reference point in the scene to be viewed are specified in line 20. The direction of the normal from the viewing window (display screen) to this reference point is specified in line 30. The position of the window about the normal is specified by line 40 and the distance of the window from the reference point is specified in line 50. Line 60 specifies the location of the observer's eye with respect to the window.*

between multiple pairs of input and plotting devices. The performance of the program suffers only a 7% degradation because of this tracking.

Asynchronous Graphics Input

Interactive graphics often uses graphics input device events to trigger an action. A Model 520 BASIC program can handle input from several graphics input devices. The operator can press the stylus or select a menu item on a digitizing tablet. These events are captured very quickly under interrupt and placed in an event queue that can be sampled later by the program. In addition, the program can specify, using an ON branch, that a particular routine is to be invoked when the event occurs. This frees the program from constantly checking the event queue for events and provides for true event-driven program design.

Extensibility

The Model 520 BASIC graphics system software is designed to separate device-independent processing from device-dependent processing. The device-independent portions of the pipeline transform output primitives to virtual device coordinates. Device-dependent drivers are concerned with the peculiarities and coordinate systems of individual peripheral devices. These drivers map the virtual coordinates into the hardware device coordinates and perform any required formatting and I/O.

This structure allows the easy addition of new device drivers. Thus, this graphics subsystem can be easily extended to take advantage of new peripherals. The recent release of the HP 97062A Color Video Interface and the HP 97060A Graphics Processor illustrates this extensibility and demonstrates the ability to support future peripherals.

High Performance

A major goal was to provide high-performance graphics. The original goal was to generate vectors ten times faster than the rate for the HP 9845C Computer of 250 vectors per second. The Model 520 Computer far exceeds this goal. Two-dimensional vectors can be generated in buffered mode at 5500 vectors/s (see Fig. 4).

Many components contribute to this performance. The Series 500 32-bit processor's speed and the vector generation rates of the HP 98770A Display for the Model 520 are essential. In addition, the performance reflects a planned tuning phase in the implementation process.

The tuning tools available to the design team included a debugger that allowed execution tracing and a software scope that provided execution time profiling. These tools were the key to minimum effort in performance tuning. They allowed detailed analysis of software performance and bottlenecks. This enabled selective tuning and recoding efforts to be concentrated on the areas that could provide the largest dividends.

The code modularity was also a contributing factor to the performance. The implementation is based on a modular design with ease of system construction, ease of maintenance, and reliability as primary goals. This same modularity permitted independent tuning of bottlenecks and experimentation with alternative algorithms and code sequences. Entire modules were rewritten without impact on the overall system. The result of this tuning effort was a sixfold performance improvement over that for the untuned code.

The generation of the viewing transformation matrix was a performance bottleneck until the tuning efforts improved the performance. Each vector endpoint is multiplied by this matrix to transform the point into virtual device coordinates. The matrix is logically constructed when the viewing operation changes by multiplying the matrices defining the component transformations to generate the transformation matrix. To reduce the time to compose this matrix, a

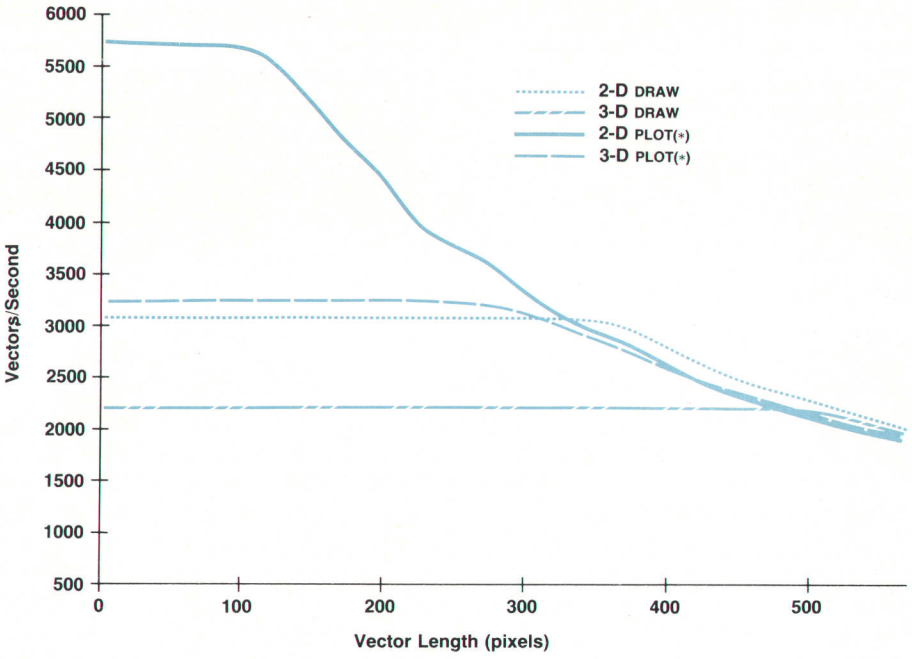


Fig. 4. *The graphics system for the desktop Series 500 Computer, the HP 9000 Model 520, provides a vector generation rate more than 20 times faster than that provided by the earlier HP 9845C Computer (250 vectors/s).*

program was written to multiply matrices defined in terms of symbolic equations. This yields a transformation matrix with individual elements expressed as equations. The values for the transformation matrix can be generated at run time by evaluation of these equations using current variable values rather than the standard matrix multiplications. These equations are simpler than the original matrix multiplication, because many terms cancel or combine. Hence, the number of required operations at run time is greatly reduced.

Reliability

The quality and reliability of the Model 520 graphics software is the result of executing a carefully thought-out test plan during the quality assurance project phase. This plan included code reading by authors and nonauthors as well as construction of test programs. Automated test programs were written to exercise all lines of code. The unattended operation of tests allowed reverification of most of the system after bug fixes. Only a few tests using operator intervention were required to extend the coverage to all of the graphics code. Several tools were developed just for the graphics software to increase the thoroughness of the tests. One tool used the special debugging instructions of the processor to generate error conditions artificially. This allows simulation of I/O errors and out-of-memory conditions to test the software error recovery and reporting. A pseudographics device driver was written that could record all data transmitted to the driver. The automated test suite compared the data recorded by this driver with previously generated data that had been checked for correctness. To ensure that the tests were in fact exercising all of the code, a coverage monitor was written that used the processor debugging instructions to measure exactly what lines of code had been executed. Tests were added to the suite based on the information gathered with this tool.

Acknowledgments

Mike Kolesar managed the project and provided technical direction. Danny Darr handled the project organization and scheduling, and implemented the graphics input and font statements. We would like to thank Jeff Eastman, who was the initial project manager and provided direction for the project, and Bill Eads, the section manager who doubled as our project manager in the interim.

References

1. R.A. Jewett and R.W. Fredrickson, "The System 45C User's Firmware Interface," *Hewlett-Packard Journal*, Vol. 31, no. 12, December 1980.

2. H.L. Baeverstad, Jr. and C.C. Bruderer, "Display System Designed for Color Graphics," *ibid.*

3. J.G. Fiasconaro, "Instruction Set for a Single-Chip 32-Bit Processor," *Hewlett-Packard Journal*, Vol. 34, no. 8, August 1983.

Multiprogramming in Model 520 BASIC

The hardware of the HP 9000 Series 500 Computers provides a high-performance, multiple-processor, 32-bit processing system. The challenge facing the designers of the BASIC software for the Model 520 Computer was to exploit the capabilities of this system fully in the form of a friendly, integrated BASIC workstation. A key objective is to increase user productivity.

To help achieve this objective, Model 520 BASIC provides a single-user multiprogramming system. This powerful feature allows the user to create and control multiple independent programming environments, called partitions. Each partition is, in effect, a virtual computer that contains its own program, data, and I/O resources, and has its own complete, independent state. Each partition can run programs, interact with the user, access all of the computer's resources and peripherals, and use all the features and statements of BASIC as though it were a complete and independent BASIC machine.

Multiple partitions enable the user to perform many different tasks concurrently. The user can use multiple partitions to develop programs while executing others, to execute several independent programs simultaneously, or to execute several cooperating programs concurrently to solve a single problem. Partitions provide a mechanism for a single BASIC user to take full advantage of the multiple-processor architecture of the Model 520 Computer.

Foreground and Background Operation

As an integrated single-user BASIC workstation, the Model 520 Computer provides a single display and keyboard. Each partition, however, has a virtual display and keyboard through which the partition interacts with the user. At any given time, only one partition is connected logically to the physical display and keyboard. This partition is called the foreground partition, while all others are called background partitions. All key inputs are directed to the foreground partition, and the foreground partition's virtual display is visible on the display. A special key on the keyboard forces the next partition in the list of existing partitions to become the foreground partition. Similarly, the current foreground partition can allow another partition to become the foreground partition via an **ATTACH** statement.

The display can be divided into logically independent sections, called screens, which can be defined as rectangular areas of a specific number of lines and characters starting at a particular position on the display. A screen has all of the display's attributes and it can be either public or private. Public screens are visible at all times. However, private screens are visible only when the partition owning them is the foreground partition. Public and private screens enable the user to print alphanumeric information to different areas of the display from various partitions with or without affecting other partitions' alphanumeric displays. Public screens are useful for displaying information about background partitions.

Screens can overlap on the display. When screens overlap, the most recently accessed screen is displayed in the overlapped area. The display update algorithm is analogous to a stack of papers in which the most recently accessed sheet is placed at the top of the stack, obscuring all overlapping sheets below.

Memory Management

The internal Series 500 operating system, called SUN,[1] manages and allocates memory to the partitions. When a partition is created, the operating system establishes a new address space for the partition and allocates an initial amount of memory for the partition. As the memory requirements for a partition's code and data change, the operating system dynamically reallocates system memory as required. Unused memory is normally reclaimed from partitions on demand for use by other partitions. However, it is possible to create a private partition that is not subject to any memory recovery procedures. When a partition is created, it is possible to specify a statement to be executed in the context of the new partition. This can be used to force a new partition to load and execute an arbitrary program.

Partition Process Model

Each partition resides in its own address space. At least two processes exist in the address space of each partition and share a user segment table, a common global data segment, and other data segments. These local data segments maintain the state of the virtual machine for the partition. The executive process executes the editor, parses user program lines and keyboard commands, manages the state of the user program, and performs any program load functions. The run process compiles and executes user programs and commands, and allocates and deallocates user variables. In addition, a human interface process buffers keystrokes and communicates with the executive process of the current foreground partition. The human interface process is a system process that attaches itself to the address space of the current foreground partition to gain access to the proper address range. Other processes are created in the partition as needed to support asynchronous I/O and timer functions. An operating system process performs memory management functions like dynamic stack extension and partition creation.

Partition Priority and Scheduling

Each partition and each process in a partition are assigned a priority. The SUN operating system allocates the CPU resources of the system to unblocked processes based on this priority. The operating system always dispatches the highest-priority process that is not blocked. In a multiple-processor system with n CPUs, the n highest-priority unblocked processes execute in parallel. Processes of equal priority share the CPU resources of the system in a round-robin manner.

Interrupt priority partitions can be created that execute at a higher priority than all other processes, even system processes. Combined with a preemptive scheduler, interrupt priority partitions provide predictability and increased performance in servicing interrupts.

Synchronization via Events and Locks

Partitions can be synchronized and resources can be managed between partitions through the use of events. Events are user-named semaphores that are globally accessible by all partitions. The operations provided by the BASIC statements **WAIT FOR EVENT** and **CAUSE EVENT** map directly onto the **DOWN** and **UP** semaphore operations used by the operating system. In addition, interpartition communication is possible through the **ON EVENT** statement, which defines an asynchronous branch to be taken whenever an event occurs in the system.

Data can be shared between partitions through the use of files. To provide high-speed access to shared data, memory resident volumes can be created. Files allocated on memory resident

volumes can be accessed without any latent device delay. Accesses to all files can be synchronized between partitions through the use of LOCK and UNLOCK statements, which ensure exclusive access to a file.

Acknowledgments

The development of the Model 520 BASIC language system related to multiprogramming was done by Jack Cooley, Harvey Clawson, Karl Freund, Dave Landers, Tom Lane, Dick Rupp, Tim Tillson, and David Wight. SUN operating system support was provided by Dan Osecky, Denny Georg, Marcel Meier, Charlie Mear, and Bob Lenk.

Reference

1. D.D. Georg, B.D. Osecky, and S.D. Scheid, "A General-Purpose Operating System Kernel for a 32-Bit Computer System," *Hewlett-Packard Journal*, Vol. 35, no. 3, March 1984.

Robert J. Bury
Software Development Engineer
Fort Collins Systems Division

I/O Features of Model 520 BASIC

by Gary D. Fritz and Michael L. Kolesar

EVEN THOUGH the HP 9000 Model 520 Computer is not targeted for the controller market, it was considered necessary to include controller-type operations in its BASIC language system. Many potential customers want to be able to read data from instruments, use the computational power of this 32-bit computer to process the data, display the data graphically, and then control other instruments using this new data. The I/O language for Model 520 BASIC was designed to fill this need.

Given these goals, several objectives were established. Of primary importance, as in nearly every other facet of the system, was performance. The Model 520 provides a tremendous computational price/performance advantage over the previous generation (the HP 9845 Computer), and the same improvement was desired for its I/O capability. Several features that were missing or difficult to use in the HP 9845 are added or improved on the Model 520. The Model 520 I/O commands were to be as compatible as possible with the earlier HP 9845 commands, while adding new I/O features and staying fully compatible with the Series 200 Computers. Last, it was important to provide an I/O language that was safe to use in a multitasking environment.

Unified I/O

Probably the most important contribution of Model 520 BASIC is the concept of unified I/O. This feature causes all I/O resources to look the same. Using unified I/O, a user's program can access a file, device, or user-defined buffer with almost no change to the program. Even different file types, which may have vastly differing internal structures, can be accessed by the same commands. For example, the Model 520 can read and write its native SDF hierarchical format discs, discs written by the HP 9825, HP 9835, and HP 9845 Computers, and those written using LIF (logical interchange format, a company-wide HP disc format) by Series 200 Computers or other systems. Data is stored in totally different ways on these disc formats, but the user's program need not be aware of this. When the program opens a file, the underlying operating system takes care of determining the disc format and file type, and manages all further interactions with the file. Later references to the file can blindly read and write data, and it is automatically reformatted as required by the target file. This may involve turning internal-format numbers into their ASCII equivalents, converting the Model 520's IEEE binary floating-point numbers into the HP 9845's BCD format, or other transformations.

This uniform interface to I/O resources is made possible by the division of I/O statements into two categories: declarative and data movement statements. The declarative statements such as ASSIGN or PRINTER IS create an I/O path identifier describing what kind of I/O resource is to be accessed, where it is located, how it is to be accessed, etc. The data movers such as ENTER and OUTPUT then use this preselected data path without worrying about its characteristics. They just specify which data path is to be used and which values are to be read or written. The I/O system then uses the attributes associated with the data path to decide how the data should be formatted, whether it should be buffered for later driver calls, whether the file system or the device drivers should be invoked, which parameters they should be passed, and so on. (See box on page 22 for examples.)

This scheme has several advantages. It allows the specification of the data path to be located in one place, making it easy to find and maintain. If at a later time the user decides to change the location or properties of the I/O resource, only a few statements must be changed. Similarly, in many cases the user can write I/O programs that do not care about the eventual target device.

BASIC Language I/O Examples

Example 1:

This example illustrates the use of the ASSIGN statement to establish the attributes to be used with a variety of device requirements. Two programs are shown: one for the HP 9845 Computer and one for the Model 520 Computer. The device requirements are:

- Device 1 on the HP-IB at select code 7 and bus address 6 requires that a carriage return—CHR$(13)—be sent at end of line, that a delay of 200 ms is needed to ensure processing of the line, and that it wants to be run SERIAL.
- Device 2 on the same HP-IB at select code 7 and bus address 4 requires the normal carriage-return line-feed sequence and no delay, but needs EOI asserted with the last character and wants to run overlapped.
- The device on select code 8 is a 16-bit parallel interface and it wants unformatted 16-bit word transfers (WHS) directly from an integer array in overlapped mode.

The following two programs show the equivalent HP 9845 and Model 520 statements.

HP 9845 Statements:

```
10 OVERLAP
  .
  .
  .
700 EOL 7; CHR$(13), 200
710 SERIAL
720 OUTPUT 7,6; "Hi there."
730 EOL 7 ! Back to default for other devices
740 OVERLAP ! Restore global mode
750 OUTPUT 7,4 USING "#,K"; "Be there!"&CHR$(13) ! Suppress EOL
760 EOI 7; 10 ! EOI with linefeed
770 OUTPUT 8 WHS, NO FORMAT; Ainteger(*)
```

Model 520 Statements:

```
10 OVERLAP
20 ASSIGN @ Busdev1 TO 706; EOL CHR$(13) DELAY .2, SERIAL
30 ASSIGN @ Busdev2 TO 704
40 ASSIGN @ Worddev TO 8; WORD, FORMAT OFF
  .
  .
710 OUTPUT @ Busdev1; "Hi there."
750 OUTPUT @ Busdev2; "Be there!", END
770 OUTPUT @ Worddev; Ainteger(*)
```

Example 2:

This example illustrates the use of the Model 520's TRANSFER statement to read ahead for an ENTER statement. The program is designed so that the TRANSFER continuously tries to stay ahead of the ENTER statement's need for data by using direct memory access input overlapping the program's computation. If successful, the ENTER process never waits for data to be brought in from disc memory. Of course, if the calculation part is short enough, the TRANSFER process still may not be fast enough to keep up. Note that the formatting of the data into internal form is done by the ENTER statement.

```
10 ASSIGN @ Inputfile TO "INPUTDATA:CS80,5,0"
20 ASSIGN @ Bufferin TO BUFFER[20000]
30 TRANSFER @ Inputfile TO @ Bufferin; EOR (COUNT 20000), END, CONT
40 DIMENSION Realx(128), Realy(128)
  .
  .
500 LOOP
510 ENTER @ Bufferin; Realx(*), Realy(*)
  .
  . (computation part)
  .
800 ENDLOOP
```

TRANSFER Statement

It is often desirable to be able to spawn asynchronous reads or writes that proceed in parallel with the execution of the user's program. This allows the program to proceed with computations involving existing data while new data is coming in. The HP 9845's solution to provide this parallelism is OVERLAP mode. This allows the use of normal ENTER and OUTPUT commands, with the program continuing as soon as the I/O transaction has been started. However, this solution is difficult to use effectively and causes additional overhead in all expression evaluation, which often slows down execution unnecessarily. Since there is no explicit user-level synchronization with the asynchronous data transfer, the I/O subsystem has to manage the synchronization itself. This involves a complex mechanism using "busy bits" associated with each user variable. When an overlapped ENTER process is initiated, all the variables to be changed by the process have their busy bits set. If the user then tries to access any of these variables before the ENTER process has completed, the program waits until the variable has been updated and its busy bit cleared. This approach requires too much overhead to check the busy bit on every access to every variable.

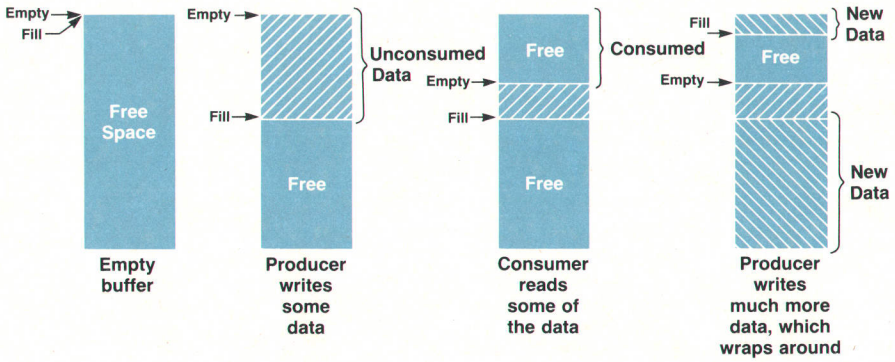
The solution adopted for Model 520 BASIC is to eliminate the overlapped ENTER and to copy the data in an overlapped OUTPUT into a temporary system buffer. This eliminates the busy bits. In addition, the TRANSFER statement was added to give the user better control over overlapped input and output. The design of the TRANSFER process permits the I/O control to stay in the low-level drivers, thereby avoiding the overhead of transaction setup and increasing throughput. As a result, properly configured TRANSFER statements can achieve continuous transfer rates of over 500,000 bytes/s to discs, and are limited only by interface speeds when talking to devices.

To use the TRANSFER statement, the user must allocate and define special buffers. These are different from the invisible, system-allocated buffers that hold data during user I/O statements. User-defined buffers are explicitly allocated and deallocated by the user, and have one other major difference: they are conceptually circular (see box on page 23). They are implemented using normal linear

Circular Buffer Operation

A sample of Fill/Empty pointer constraints which yield circular buffer behavior (see diagram).

1. Empty and Fill point to the next byte to be read or written.
2. Empty is not allowed to pass Fill.
3. The buffer is empty when Empty = Fill and Full = False.
4. The buffer is full when Empty = Fill and Full = True.
5. The buffer is reset when Empty = Fill = 0 and Full = False.
6. The buffer contains (Fill − Empty) mod N + N[(Fill = Empty)·Full] unconsumed bytes, where N is the buffer size in bytes and the expression in square brackets is equal to 1 when the buffer is full and zero otherwise.
7. When Empty or Fill would increment past N−1, they are wrapped back modulo N by successively subtracting N to keep them in the range 0 to N−1.



memory, but the I/O system manages buffer reads and writes so that the user never sees the end of the buffer. If a program tries to write past the end of the linear memory in a buffer, the I/O system automatically stops the write at the end of the buffer and resumes writing at the beginning of the buffer. This is an extremely useful feature when a program needs to pass data between a producer process and a consumer process. The producer can write data into the buffer, and the consumer can read data out of the buffer. This is managed by maintaining two buffer pointers, called Fill and Empty, which are advanced by the producer and consumer, respectively. The I/O system guarantees that these two pointers can never cross each other; that is, if the producer writes data into the buffer faster than the consumer can read it, the Fill pointer runs into the Empty pointer and the producer then waits until the consumer has read some of the data and advanced the Empty pointer. Similarly, if the consumer reads data faster than the producer can supply it, the Empty pointer runs into the Fill pointer and the consumer then waits until more data is available. This feature and the circular structure of the buffer allow continuous data transfers without worrying about running out of buffer space.

User-defined buffers are used as intermediate data storage for the TRANSFER process. Once allocated and described using the ASSIGN statement, access to a buffer looks just like access to a file or device. The main difference is that instead of accessing a device directly, an ENTER or OUTPUT command reads or writes data into the buffer allocated for the device. A TRANSFER command performs the physical I/O between the buffer and a device or file. For example, an OUTPUT statement, acting as a producer, could write data into a buffer. The data is already formatted as specified by the ASSIGN statement. The TRANSFER process, a consumer, then copies the data in the buffer to the target device or file using high-speed, low-overhead methods. The same example works in reverse with an in-bound TRANSFER and an ENTER statement; the TRANSFER process is then the producer and the ENTER statement consumes the data in the buffer. In this fashion the user can very easily implement a read-ahead scheme by transferring data into the buffer while the program is doing other work, and entering from the buffer when the program needs the data, or outputting to a buffer and letting a TRANSFER statement do the actual I/O while the program continues. (See the second example in the box on page 22.)

If no data reformatting is required, it is also quite easy to set up a two-ended transfer. In this case, one TRANSFER statement reads from a device or file into a buffer, and another TRANSFER statement writes the data in the buffer out to another device or file.

The user has extensive control over how the TRANSFER process synchronizes with the rest of the program. The process can cause end-of-record (EOR) signals on user-definable boundaries such as character count, character match, end of file, or EOI (end or identify) on the HP-IB (IEEE 488). These EOR signals, along with the user-definable end-of-transfer (EOT) signal, can be used to tell the program when to read from or write to a buffer. The user's program can either continue to do other work and optionally be notified of these signals via the asynchronous BASIC ON branching statements, or wait for one of the signals, thereby consuming no additional CPU time.

In an asynchronous multiprocess environment such as that presented by TRANSFER or by BASIC partitions, it is crucial to ensure that the various processes cooperate in their use of I/O resources. Model 520 BASIC has adopted a simple strategy to make sure that the user can write simple multiprocess applications without fear of destructive interactions. Each I/O statement, regardless of the number of

operating system calls required to satisfy it, is considered an "atomic" operation. That is, it is uninterruptable. Other processes trying to access the same I/O resource must wait until the statement has completed. If exclusive control is required over a longer term, there are several facilities (file locking and EVENTs) that can be used to synchronize and control access to a resource for any desired length of time.

I/O Performance

The I/O group was faced with many challenges when trying to achieve a performance improvement comparable to the rest of the Model 520 BASIC system. No technological breakthroughs such as run-time compiling were available. Unlike the HP 9845 and HP 9000 Series 200 Computers, the separate operating system[1] for the HP 9000 Series 500 Computers was not specifically designed for the short transactions needed by controllers. In addition, the Series 500 has a greatly expanded feature set and more complex semantics than its controller cousins, and hard experience has proven that "There is no such thing as a free lunch!" In spite of these challenges, the group was able to achieve 10× faster performance compared to that of the HP 9845, with even greater speed when the multichannel DMA hardware of the Series 500 is fully exploited.

Transportation to Other Computers

Compatibility with other HP products was a major goal of the entire Model 520 BASIC project. It was recognized that many HP 9845 customers would want to upgrade their applications to the Model 520 for its increased capacity, computational power, and multitasking environment. Hence, a simple transportation path was desired. Many I/O statements had to be changed radically to implement the declarative/data-mover philosophy, but great effort was expended in many other areas to make transportation as easy as possible. Some examples include the PRINT USING/IMAGE formatting facility, which was expanded but remains a superset of the HP 9845 BASIC commands, inclusion of difficult-to-translate statements such as READ#/PRINT#, and support of the HP 9845 disc format and file types. In addition, many I/O statements and functions are translatable by the Model 520 translator.[2]

Considerable effort was also expended to maintain complete compatibility with the Series 200 Computers (HP 9000 Models 216, 226, and 236). BASIC standardization committees spent many hours to ensure that, barring hardware dependencies such as interface register bit assignments, the semantics of both systems were as identical as possible. As a result of this effort, and thanks to the ability of the Series 500 to read the Series 200's LIF discs, it is almost always possible to take a disc from a Series 200 Computer to a Series 500 Computer, GET a program, and run it without change.

Acknowledgments

In retrospect, it is somewhat amazing to members of the I/O group that so much was accomplished in so little time with so many conflicting goals and constraints. Many people deserve credit: Wayne Covington and John Harwell were part of the main development team, Dan Osecky designed the initial TRANSFER implementation, Karl Freund helped greatly with the design and implemented the closely related mass storage statements, and Jack Cooley, Dave Palermo, Kathy Kwinn, and Steve Schink worked on the common BASIC language standard used by the HP 9000 Computers.

References

1. D.D. Georg, B.D. Osecky, and S.D. Scheid, "A General-Purpose Operating System Kernel for a 32-Bit Computer System," *Hewlett-Packard Journal*, Vol. 35, no. 3, March 1984.
2. G.L. Shults, "Preserving Programming Investments," *ibid*, pp. 20-21.

A Compact, Reliable Power Supply for an Advanced Desktop Computer

by Jack L. Burkman, Howell R. Felsenthal, Thomas O. Meyer, and Warren C. Pratt

BECAUSE THE HP 9000 MODEL 520 COMPUTER has several configurations, a key design goal for its power supply module was provision for flexibility in output currents and power. These configurations include the various combinations of CPU, I/O processor, and RAM finstrates that can be installed in the twelve slots of the Model 520's Memory/Processor Module and the set of internal peripherals. The set of peripherals can include up to four I/O adapters, two mass memory devices, a high-speed thermal printer, a keyboard, and a graphics display subsystem. These widely varying configurations, in addition to requiring large variations in total output power, greatly affected the design of individual supply outputs. If all required supply outputs were simultaneously loaded to their maximum current ratings (a hypothetical load), the total output power required would be about 830W.

Other key design goals included a power density commensurate with the volume available in a desktop worksta-

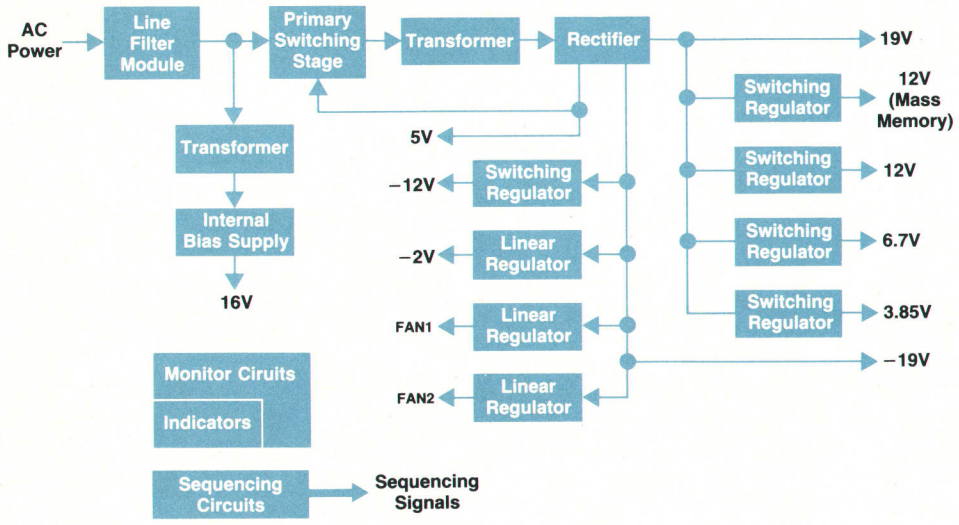


Fig. 1. *Block diagram of the power supply module for the HP 9000 Series 500 Computers.*

tion, regulation and output protection consistent with the requirements of the NMOS-III VLSI technology used for the 32-bit chip set, compliance with HP's Class B environmental specification for industrial and commercial environments, and high reliability.

The resulting power supply module developed for the Model 520:

- Supplies up to 550 watts divided in a configuration-dependent manner among 12 outputs (10 of these are precisely regulated)
- Monitors and protects all outputs
- Provides power-up sequencing for the remainder of the machine
- Meets stringent environmental and regulatory specifications
- Has a power density of 1.4W per cubic inch.

This power supply is also used in other HP 9000 Series 500 Computers.

The electrical topology of the power supply is shown in Fig. 1. The ac line filter module provides ac power to a full-wave-bridge primary switching regulator circuit whose outputs are 5V (regulated) and ±19V (unregulated). The 5V supply serves as the main logic supply voltage for the Model 520 while the two unregulated outputs are for subassemblies that either do not have stringent regulation requirements or provide their own regulation. The 19V and −19V outputs also serve as raw supplies from which many other regulated supplies are derived. Four outputs, 3.85V (used by NMOS-III ICs), 6.7V (NMOS-III ICs), 12V (NMOS-III and other logic ICs), and 12V (mass memory), are developed from the 19V output using switching regulators. Three outputs, −2V (NMOS-III ICs), FAN1 (fixed-speed dc fan supply), and FAN2 (variable-speed dc fan supply) are developed from the −19V output using linear regulators and a −12V logic output is developed using a switching regulator.

The drive circuits for the primary switching regulator and the sequencing and monitoring circuitry are powered by an internal 16V bias supply. This 16V supply is available as a low-current output in the Model 530 and Model 540 Computers. Outputs are individually monitored for overvoltage and undervoltage, temperatures are monitored in the Series 500 Memory/Processor Module and the power supply, and other conditions such as open access doors are checked and individually reported. Seven logic signals to control power-up and power-down operation are provided by the sequencing circuitry.

Mechanically, the supply is divided into two indepen-

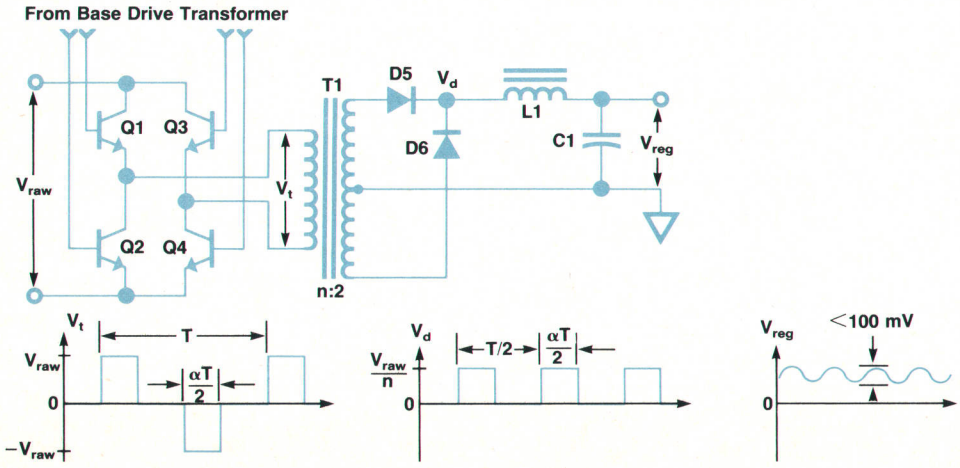


Fig. 2. *Basic circuit diagram of the primary switching regulator circuit. See Fig. 3 for more details.*

dent modules, the line filter module and the power supply module. The line filter module contains the ac line filter, circuit breaker, and associated wiring. The power supply module consists of three printed circuit board assemblies and two major heat sink assemblies. The primary board contains the primary switching regulator, the 5V output circuitry, and the internal 16V bias supply. One heat sink assembly is attached to this board to cool the four primary switching transistors. The secondary board houses the ±19V output circuitry and the five remaining switching regulators. The other heat sink assembly is attached to this board to cool the ±19V rectifiers and the power devices for four switching regulators and the −2V linear regulator. The supervisor board contains monitoring and sequencing circuitry as well as the linear regulators for the two dc fan supplies, FAN1 and FAN2.

Primary Switching Regulator

A simplified diagram of the primary switching regulator circuit is shown in Fig. 2. V_{raw}, nominally 305Vdc, is an unregulated voltage derived from the ac line voltage by rectification and filtering. Transistors Q1 through Q4 are driven to conduct in pairs to apply plus and minus V_{raw} alternately across the primary winding of transformer T1. This voltage waveform (V_t), known as a pseudosquare wave, is stepped down by T1 and rectified by diodes D5 and D6 to create a pulse train of frequency 2/T, duty cycle α, and magnitude V_{raw}/n. The filter elements L1 and C1 smooth the waveform, producing a dc voltage $\alpha V_{raw}/n$. Since the filtering is not perfect, there is a small ac voltage superimposed on the dc level. This ripple is limited to less than 100 mV peak-to-peak. The output voltage V_{reg} is regulated by adjusting the duty cycle of the pseudosquare wave (V_t) to compensate for changes in V_{raw}. The transformer's turns ratio was selected so that the output remains regulated over a wide variation in V_{raw}.

The main advantage of a switching supply is efficiency. Because its semiconductor devices are either on or off, little power is lost in regulation. Another advantage is size. The heat sinks can be smaller because of the efficiency, and smaller transformers and inductors can be used because the switching frequency is high. The 29-kHz switching frequency used in the supply reduces the volume of a transformer capable of handling over 600W to less than 11 cubic inches.

Unfortunately, the large voltage swings and current levels produced in switching supplies can introduce component stresses and electrical noise that make poorly designed supplies unreliable. For this power supply, much care has been taken to avoid the traditional switching supply design pitfalls. Particularly, attention was given to anything that might cause a switching transistor to fail.

The most common cause of transistor failure in this type of switching supply is simultaneous conduction. This is a transient condition in which both Q1 and Q2 or Q3 and Q4 are on at the same instant. Since this effectively short-circuits V_{raw}, destructive current levels are easily attained in the devices. Several measures have been taken to avoid this problem. First, the control circuitry provides a minimum off time of 2.5 μs between conduction periods as the duty cycle nears 100%. Second, a voltage-sensing circuit turns off the drive to the bases of Q1 through Q4 when the internal 16V bias voltage supply drops below about 13V. This eliminates the possibility of simultaneous conduction or insufficient base drive during power-up or power-down. Finally, sources of noise that could affect proper control-circuit operation are shielded, filtered, or eliminated.

In Fig. 3, the basic regulator circuit is redrawn to show the additional circuitry on the supply's primary board. Because T1, like all transformers, is far from ideal, several additions are made to the basic circuit to ensure reliable

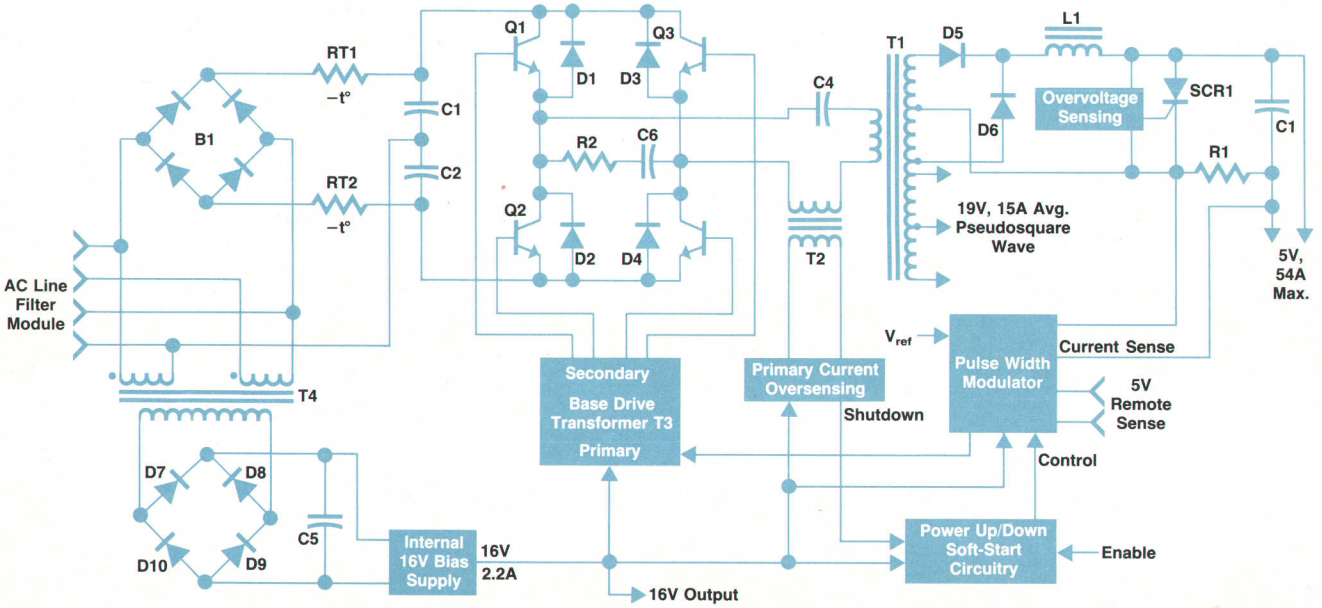


Fig. 3. *Primary regulator circuit.*

operation. First, diodes D1 to D4 clamp the transients caused by the inductance of T1. Second, capacitor C4 blocks the flow of direct current into the primary winding of T1. Without C4, T1 could become saturated, reducing its efficiency and greatly increasing the peak currents conducted by the primary switching transistors. Finally, the switching load line is shaped by R2 and C6 to reduce the amount of power dissipated in Q1 to Q4 during switching.

Line Voltage Selection. Either of two ac line voltage ranges can be used by selecting the proper line filter module. The 90-to-125Vac module is wired so that rectifier bridge B1 acts as a voltage doubler and the primary windings of T4 are in parallel. The 198-to-250Vac module configures B1 as a full-wave rectifier and connects the primaries of T4 in series. This leaves the voltages on capacitors C2, C3, and C5 about the same in either range.

Protection. An important feature of the primary switching regulator design is the protection scheme. The following types of protection are provided:

- Input overvoltage protection in the 120Vac line filter module. A gas discharge tube that acts as an open circuit during normal operation is connected across the ac line. If a Series 500 Computer configured for 120Vac operation is plugged into a 220Vac outlet, the discharge tube starts arcing, thus tripping the machine's circuit breaker.
- The 5V output current is sensed across R1 and is limited to 54A by the pulse width modulator circuit.
- The switching transistors Q1 to Q4 are protected from excessive currents by an overcurrent sensing circuit. Current flowing into the primary winding of T1 is sensed through current transformer T2 by this circuit, and if the peak current exceeds 11.4A, the primary regulator is turned off. This protects against shorts on the 19V or −19V outputs and large transient loads on the 5V output.
- Loads are protected from some power supply malfunctions by the overvoltage sensing circuit and SCR1. If the 5V output voltage exceeds a safe level, it is shorted by SCR1, which trips the primary overcurrent mechanism.
- Like the 5V output, the internal 16V bias supply (which is a switching supply) also has current-limit and overvoltage protection.

In power supplies of this size, start-up currents can be enormous if not properly controlled. This supply module uses thermistors and a soft-start circuit to limit these inrush currents. This reduces stresses on fuses and circuit breakers when a Series 500 Computer is turned on. Thermistors RT1 and RT2 limit the flow of current into C2 and C3 when power is first applied. As they conduct, they quickly heat up and their resistance becomes negligible. Shortly after C2 and C3 are fully charged, the pulse width modulator begins operating. The soft-start circuit controls the duty cycle to bring the output slowly into regulation, avoiding overstressing the components.

Secondary Outputs

The key design goal for the secondary board was to provide eight outputs and 325 watts of output power in a volume of 106 cubic inches. Six of these outputs require tight regulation and, of these, four are at high current levels. Switching regulators are used for the high-current outputs to minimize dissipation and maintain tight regulation without sacrificing reliability.

The basic series-switching regulator and associated power switch circuit are shown in Fig. 4. Transistor Q1 is alternately turned on and off with the timing duty cycle controlled to provide the desired output voltage V_o. The input voltage V_i is applied to one end of the inductor (node A) during the on period of Q1. The current I_L in inductor L1 increases linearly until Q1 is turned off. To maintain current flow through L1 during the off period, node A goes negative causing the "catch" diode D1 to conduct. This allows I_L to decrease linearly until Q1 is again turned on. If the inductance is large enough to maintain current flow during the off period, the output voltage is

$$V_o = V_i T_{on} / (T_{on} + T_{off}) = V_i \times (\text{Duty Cycle})$$

The inductance required to satisfy this condition is inversely proportional to load current and switching frequency. Because the load current I_o is supposed to be constant, the ripple current in L1 (i.e., the ac component) is shunted to ground by output capacitor C1. This ripple current contributes to output ripple voltage because of the equivalent series resistance, or ESR, of the capacitor. The ripple current is inversely proportional to both the inductance and the switching frequency.

A high switching frequency reduces output ripple and the required inductance. However, a switching transistor with nonzero turn-on and turn-off times dissipates power at each transition. This dissipation is proportional to switching frequency. Design of a compact yet efficient series switching regulator requires careful tradeoffs between switching frequency, inductor value, capacitor ESR, and the minimum load current.

The power switch is a critical element in a switching regulator. For low dissipation it must have a small dc voltage drop in the on state and fast switching speed. A rugged switch is crucial to the reliability of such a regulator. The high-current secondary regulators use the switch circuit shown in Fig. 4. When the output of the pulse width modulator is low, it turns on Q3, Q2, and then Q1. Because transistor Q1 never goes into deep saturation (v_{bc} of Q1

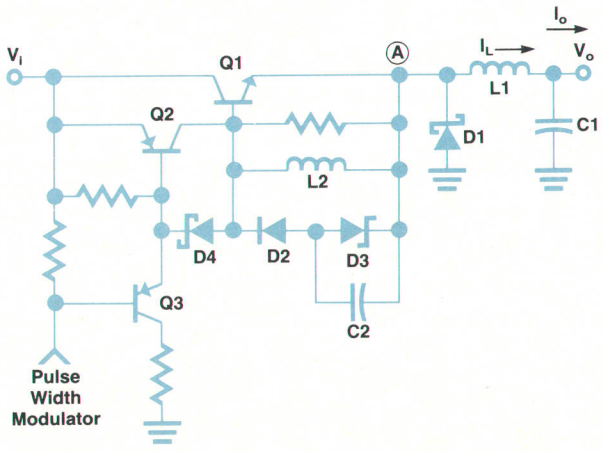


Fig. 4. *Basic series-switching regulator and power switch circuits.*

An Automated Power Supply Test Station

In the past, automated power supply testing has been difficult or impossible to do because of high currents and hazardous voltages. For the supply used in the HP 9000 Series 500 Computers, a completely automated test station was developed. This station is capable of testing either individual boards or a completed power supply assembly under in-circuit conditions.

The test station uses HP-IB (IEEE 488) instruments and a custom test fixture under the control of an HP 9000 Model 226 Computer (Fig. 1). It performs more than 150 power supply tests in a fraction of the time required to do them manually. If a supply fails a test, the test station provides a printout listing the test, limits, and measured values to simplify troubleshooting. Test modifications can be done by a simple software change and failure rate statistics are easily collected. In addition, the Model 226 provides a friendly, interactive user interface which allows an operator to monitor system status or if necessary, to set test parameters for troubleshooting.

The test fixture is the heart of the system. It contains the solid-state on/off relay, the 110/220V line voltage selection relay, and the high-current relays to connect loads to the supply outputs. Variable line voltage is provided by a motor-controlled variable autotransformer. With this variable line voltage, the supply can be tested in both voltage ranges automatically. Output loading up to 300W is done with a programmable load. Each power supply output can be connected to the load by the high-current relays in the test fixture to check current limits and voltage regulation. Additional fixed loads contained in the test fixture are used with the variable load to test the supply at its rated capacity. External stimuli for checking the protection circuitry and for powering small sections of the supply while the main switching supply is off are provided by a programmable HP 6002A Power Supply.

Line voltages, digital signal levels, and dc and ripple voltage values are measured by an HP 3456A Digital Voltmeter. An HP 5316A Universal Counter measures the operating frequency of the supply and the sequencing of the power-up signals on the supply's monitor board. An HP 3497A Data Acquisition/Control Unit multiplexes the signals to be measured and controls the functions of the test fixture.

To do a test, the operator simply plugs the power supply into the fixture and presses the appropriate softkey on the Model 226. In minutes the test is complete, the results are printed, and the fully tested supply is ready for use.

Thomas O. Meyer
Development Engineer
Fort Collins Systems Division

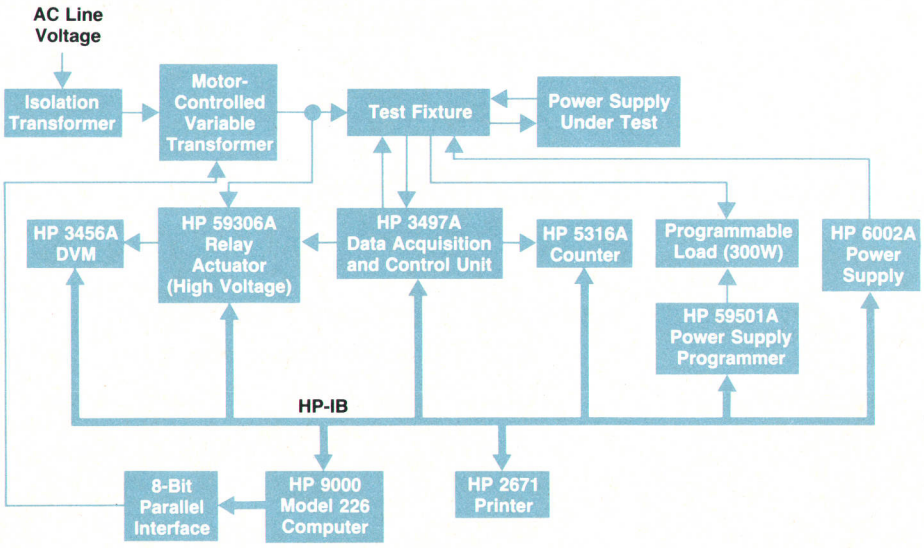


Fig. 1. *This automated test station is a custom system controlled by an HP 9000 Model 226 Computer that automatically tests the power supply modules used in HP 9000 Series 500 Computers.*

cannot be less than v_{ce} of Q2), storage and fall times are improved. The turn-off time of Q1 is further improved by connecting inductor L2 from its base to its emitter. During the on time, current increases linearly in L2. When Q2 turns off, the voltage across L2 reverses, drawing stored charge out of Q1's base junction. Diodes D2 and D3 and capacitor C2 clamp the voltage across L2 to prevent reverse breakdown of Q1's base-emitter junction.

A narrow pulse width is required to convert 19V to 3.85V. For this regulator, Q2 is clamped by Schottky diode D4. This prevents deep saturation of Q2 and improves overall turn-off time at the expense of a higher dc voltage drop across Q1. The speed of this power switch allows operation at 60 kHz without excessive power loss.

An important design goal was to minimize the consequences of a failure. That is, a Series 500 Computer should be protected from a fault in its power supply. Analysis showed that suddenly short-circuiting a switching transistor could drive an output to over 25 volts for several milliseconds even if the primary switching regulator is turned off instantly. This is a result of energy storage in the 19V supply capacitors and the presence of the output inductor. Crowbar circuits on all switching regulators on the secondary board prevent this from happening. These circuits consist of an SCR and a control IC on each output. If an output exceeds a set level, the associated SCR is triggered, short-

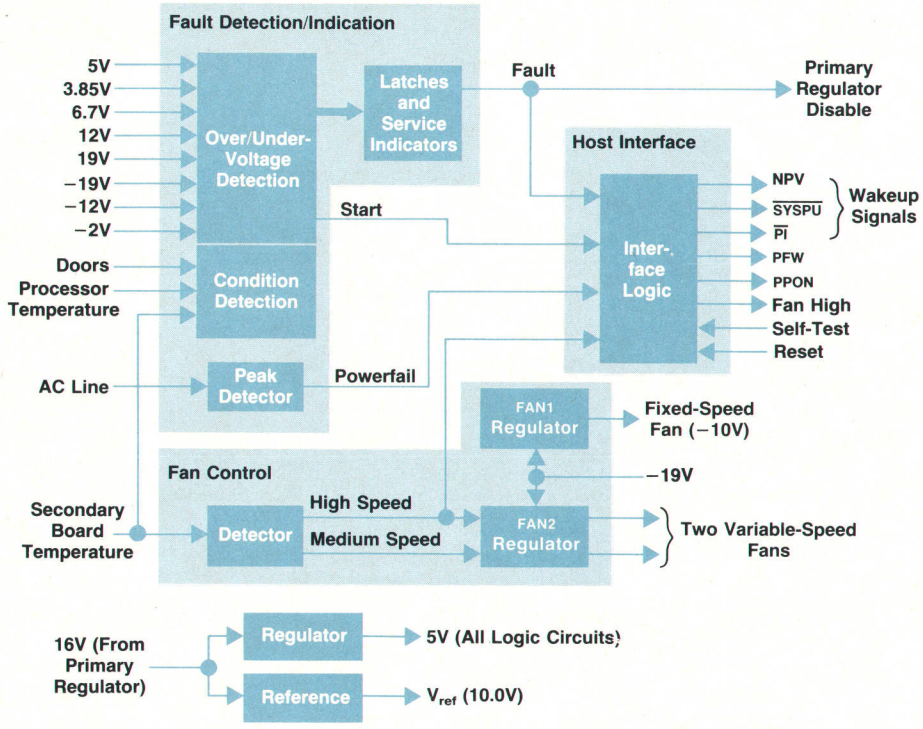


Fig. 5. *Block diagram of supervisor board.*

circuiting that output to ground. The crowbar circuits also provide protection against a short circuit between supplies anywhere in the computer.

Complementing the crowbar circuits, each regulated output has a current limit. These protect the regulators from overload and prevent damage when a crowbar circuit is triggered.

Supervisor Board

The supervisor board, as the name implies, monitors operation of the entire power supply. In addition, it controls the three dc cooling fans and provides seven logic signals to the mainframe. The major sections of the supervisor board are shown in Fig. 5.

The supervisor fault detection system plays a key role in protecting a Series 500 Computer from power supply failures. In addition to undervoltage and overvoltage sensing, it monitors door interlocks and the temperature of the Memory/Processor Module. If any fault occurs, the primary switching regulator is immediately turned off. While this level of protection may not be unusual in large computer power supply systems, it can make servicing difficult if the supply continues shutting itself off. As an aid to servicing, the supervisor board displays the cause of a shutdown on lights in the top cover of the supply module. To latch and drive the appropriate lights for 18 different fault conditions economically, a gate-array circuit is used.

Regulators for the three dc fans are also on the supervisor board. A single regulator (FAN2) powers two of the fans for low-, medium-, or high-speed operation. Speed selection is based on the temperature monitored by a thermistor mounted on the secondary board's heat sink. This large heat sink carries all the rectifiers, catch diodes, and pass transistors except for the −12V output circuit. Dissipation on this heat sink is roughly proportional to the total power drawn. When the fans are switched to high speed, a signal is sent to the host processor to inform the user of this condition. The third fan is powered by a fixed-voltage regulator (FAN1) and operates at low speed.

Two other supply status signals are sent to the host processor. PPON indicates that output voltages are in regulation. PFW signals impending loss of output voltage regulation, allowing the computer time to enter an idle state.

In addition to providing status information, the supervisor board is responsible for waking up the host processor. The NMOS-III Memory/Processor Module used in the Series 500 Computers requires three signals, properly synchronized, to begin operation at power-up. The supervisor board uses a ROM state machine to generate this sequence.

Mechanical Structure

The power supply has five major elements: three printed circuit boards and two heat sink assemblies. These ele-

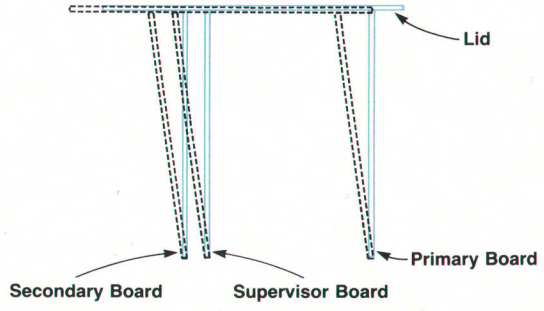


Fig. 6. *The flexibility of the power supply module's mechanical structure allows a slight angular distortion (exaggerated here for clarity) to reduce shear stresses on the connectors.*

ments are stacked together in a manner similar to an old clock mechanism. In such a clock, top and bottom plates capture meshed gears to provide an assembly that is dependent on adjacent elements for alignment and support. In the Series 500 power supply module, each element plays a similar role in providing structural support for adjacent elements. In addition, cooling air flow is diverted to areas of high power density by the interaction of these elements.

The three printed circuit boards are mounted vertically. This arrangement minimizes problems associated with moisture condensing on the boards in high-humidity conditions and allows logical routing of the power lines. A cable routes the ac line voltage from the line filter module to the top of the primary board. Three brass bars conduct the 19V pseudosquare wave from the primary board to the secondary board. All other power and signal lines are routed to the computer's motherboard and then to the appropriate board within the power supply or to the appropriate module within the computer.

The completed power supply resides in a sheet-metal "bucket" within the Series 500 Computer. To ensure reliable connector engagement during insertion into this bucket, a three-step alignment method is used. The plastic board spacers attached to the end of the supply provide a gross guide against the side of the bucket. When the connectors are about 15 mm from engagement, pins attached to the computer's motherboard engage receptacles attached to the primary board and the secondary board. This brings the connectors to within 2 mm of the correct position. When the connectors are about 5 mm from engagement, details molded into the connector housings complete the alignment.

Once the connectors are fully seated, captive screws attached to the lid are tightened. These screws are free to float along the longitudinal axis of the power supply. This ensures that connector pins and contacts are not subject to a shear stress. The screws are not free to float perpendicular to the longitudinal axis. In this direction the completed assembly is designed to allow its shape to change slightly from a rectangle to a parallelogram (Fig. 6). This creates a very small angular mismatch between the connector pins and the connector contacts while minimizing any shear loading. (This angular mismatch is small compared to the angle variation occurring during production assembly and soldering of the connectors.) Connector pin-to-contact engagement is statistically designed to ensure that the power supply connectors will reliably engage the mating connectors in the mainframe.

The power supply is produced as an independent module and is fully tested before installation. Once installed, the supply can withstand 0.38-mm amplitude vibration at 5 to 55 Hz for a sustained period while remaining fully functional. It can also withstand a 30g, 11-ms half-sine-wave shock in any axis without damage.

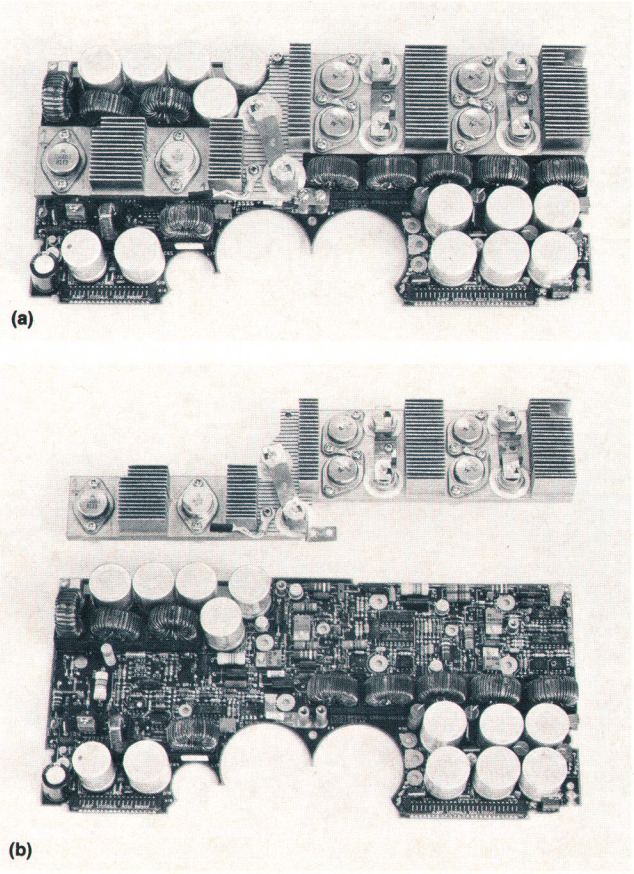


Fig. 7. *Secondary board assembly. (a) With common heat sink assembly installed. (b) With heat sink removed.*

Cooling

To improve reliability, device junction temperatures should not exceed 80% of the maximum junction temperature rise specified by the manufacturer at 4570 m altitude and 55°C. In a typical environment of 25°C at sea level, device temperatures should be maintained below 50% of the maximum junction temperature rise. In designing the cooling for the power supply module, thermal derating proved to be the greatest design challenge since up to 300W is dissipated inside a volume of less than 400 cubic inches.

Early modeling of the design, using paper models of the boards and individual elements, allowed the air flow channels to be optimized. The primary and supervisor boards enclose the first chamber. The second chamber is created by the secondary board and the sheet-metal bucket wall. These chambers are sized so that the air exiting both cham-

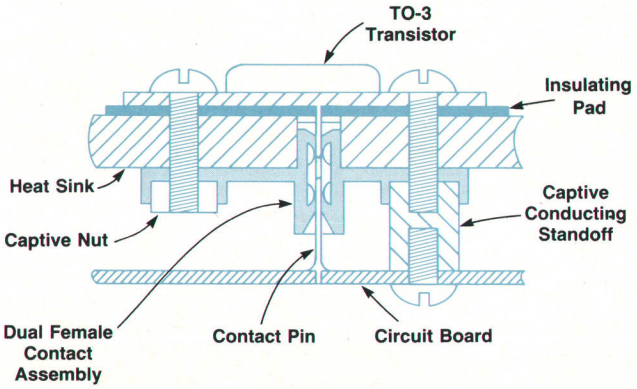


Fig. 8. *A custom connector is used to connect the power transistors on the secondary board's heat sink to the secondary circuit board.*

bers is the same temperature. The dc fan located at the rear of the power supply evacuates the power supply module. The fan speed varies according to ambient temperature, altitude, and load on the secondary board outputs.

The greatest packaging and cooling challenge occurred on the secondary board (Fig. 7). The large number of components and high thermal load dictated the design of a very compact and efficient heat exchanger that was easily assembled. Individual power devices on the secondary board can vary in thermal dissipation from one watt to greater than 17 watts, depending on the load configuration supported by the power supply. If discrete heat sinks loaded to their maximum current ratings (a hypothetical load) were used, there would be 12 heat sinks dissipating more than 90W. By placing all major power devices on one heat sink, individual devices do not have to be cooled for their worst-case power dissipations. Instead, the common heat sink thermally links the devices so that increased power dissipation in one device can be offset by decreased power dissipation in an adjacent device. The common heat sink can dissipate 75W under worst-case conditions.

The common heat sink assembly consists of six power diodes, five power transistors, one regulator, custom connectors, and a swaged heat sink. The heat sink is formed by piercing, blanking, and machining a metal extrusion. Many shallow slots parallel to the longitudinal axis are formed into one side of the extrusion. Stamped aluminum plates are inserted into the slots and the sides of the slots are deformed or swaged into the plates. This creates an economical heat sink that has five separate banks of heat exchanger plates (see Fig. 7). The short length of each of these rows minimizes the growth of the air boundary layer and optimizes the heat dissipation ability of the heat sink. The 6-mm thick base of the extrusion ensures a minimal temperature difference between devices regardless of power dissipation. The thermistor that provides temperature sensing for the fan control circuit is mounted in the middle of this heat sink.

The power transistor packages are attached to the heat sink with a custom connector (Fig. 8). The connector is an injection-molded piece that encapsulates a double female contact. The transistor leads are first inserted through an electrically insulating but thermally conductive pad, then through the heat sink, and finally into the connector. A screw is inserted through the transistor case flange into a nut or standoff held captive by the connector. This provides the clamping force necessary to ensure a low thermal impedance path from the device to the heat sink. The diodes are attached to the heat sink with another electrically insulating pad and a custom plastic washer. The diode stud is inserted through the pad, heat sink, and washer, and into a threaded standoff held captive by the washer. (The washer is pinned to the heat sink to prevent rotation of the standoff.) Brass stampings are soldered to the diode terminals and self-tapping screws attach them to the heat sink. This provides a self-contained module that can be simply plugged into the secondary board.

As the heat sink assembly is plugged into the board, guide pins attached to the secondary board ensure that the connectors to the transistors on the heat sink are able to engage pins soldered to the board. The connectors have a molded detail that completes the guiding and ensures that the pins are not damaged.

A similar heat sink module is used for the four primary switching transistors on the primary board. This heat sink is formed using a conventional fin extrusion and a drilled base. The main filter capacitors constrict the cross-sectional area of the primary/supervisor board chamber to increase the air velocity over this heat sink.

Acknowledgments

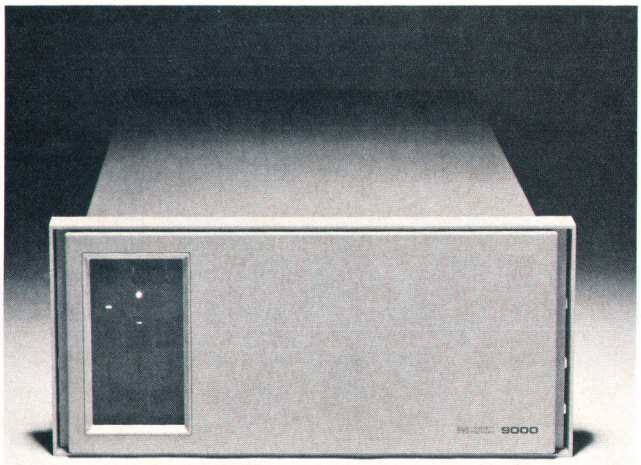
We wish to thank Gary Seldner and Dave Post for their technical contributions to the design, Paul Febvre for his guidance in mechanical design, and Jim Latimer and Charlie Rock for their work in prototyping and testing.

Compact 32-Bit System Processing Units

by Kevin W. Allen, Paul C. Christofanelli, Robert E. Kuseski, Ronald D. Larson, David Maitland, and Larry J. Thayer

HEWLETT-PACKARD'S proprietary VLSI NMOS-III technology allows the integration of an entire 32-bit central processing unit (CPU) on one chip.[1] This technology has enabled HP to build high-performance 32-bit computers that can be adapted to the customers' environment rather than forcing users to adapt to an environment that meets the computer specifications. An operating temperature range of 0°C to 55°C, use of standard ac line voltages, and EMI (electromagnetic interference) certification allow the Model 530 and Model 540 System Processing Units (SPUs) of the HP 9000 Series 500 Computer family to be used in a broad range of environments. In addition, thorough testing was done to ensure that these SPUs and their peripherals would work properly in the presence of EMI and electrostatic discharge (ESD).

Two packaging styles offer adaptability to customer needs. The Model 530 fits into an industry standard rack (Fig. 1a). The Model 540 matches a wide selection of HP computer peripherals (Fig. 1b and Fig. 2). Both models include a 32-bit CPU, I/O processor, I/O card cage, power



(a)

(b)

Fig. 1. *The HP Model 530 (a) and Model 540 (b) System Processing Units are based on HP's proprietary 32-bit VLSI NMOS-III circuits. The Model 530 is designed for rack-mount configurations and the Model 540 is designed for use in office system environments (see Fig. 2). These two processing units, like other members of the HP 9000 Series 500 family, can have more than one CPU and one I/O processor for applications requiring the added performance. Both units can be programmed and networked using HP's HP-UX and LAN 9000 systems.*

supply, real-time clock, and hardware self-test. System performance and capabilities can be altered to meet individual requirements by adding more CPUs for more performance, more RAM for more memory space, or more I/O processors for additional I/O cards. These SPUs can be configured with either single-user or multiuser HP-UX operating systems.

Architecture

The internal architecture of both models is shown in Fig. 3. The major architectural block is the Series 500 Memory/Processor Module,[2] which contains the CPU, RAM, and I/O processor (IOP) for the SPU. Each functional subunit of the Memory/Processor Module is contained on a single copper-core "finstrate," which provides interconnect and thermal dissipation for its IC chips.[3] These finstrates are connected via the memory processor bus (MPB) inside the Memory/Processor Module. This bus provides a 36M-byte/s communication path for the finstrates in the stack.

The circuitry on the finstrates is based on a VLSI chip set built with HP's NMOS-III technology.[4] This technology provides almost 500,000 transistors on a single chip through the use of 1.5-μm-wide metal interconnect lines with 1.0-μm spacings. The chip set includes CPU, IOP, memory controller, 128K-bit RAM, and clock buffer chips, which are mounted and bonded directly to the finstrates. All of the chips run with an 18-MHz, nonoverlapping clock.

The CPU finstrate contains a single-chip 32-bit microprocessor with a 9K × 38-bit microcode instruction set cycling with a 55-ns period. Each I/O processor supports up to eight I/O channels with direct memory access (DMA) capability on each channel. Each RAM finstrate has a memory controller chip that provides correction for single-bit errors and detection of double-bit errors. All of this is done with a pipelined architecture that achieves a 110-ns RAM cycle time. SPU performance and capabilities can be tailored by selecting various configurations of up to twelve finstrates for the Memory/Processor Module.

The first IOP finstrate controls the SPU's internal I/O bus. The I/O bus is connected to the system control module and seven internal I/O card slots via the backplane. Any combination of HP 9000 Series 500 I/O cards can be used in these slots to provide the desired I/O function. Up to two I/O expanders (HP 97098As) with eight I/O slots each can be supported by adding one IOP finstrate to the Memory/Processor Module for each expander.

The system control module performs control and support functions for the SPU. The control module contains:

- Service-panel control circuits
- The loader ROM
- A real-time clock with battery backup
- 2048 bytes of nonvolatile memory
- The system status interface to the CPU.

The loader ROM contents are loaded into main memory and executed at power-up. The code instructs the CPU to do some internal self-testing and to load the operating system. The real-time clock with battery backup has an accuracy of 30 seconds per month (typical) and will keep time for one month when the power is turned off in a normal environment. The nonvolatile memory is used for storing such useful information as the number of times power has been cycled and the number of accumulated hours of SPU use. The system status interface relays information such as powerfail warnings, high-temperature warnings, and the nonmaskable interrupt status of the I/O backplane to the CPU.

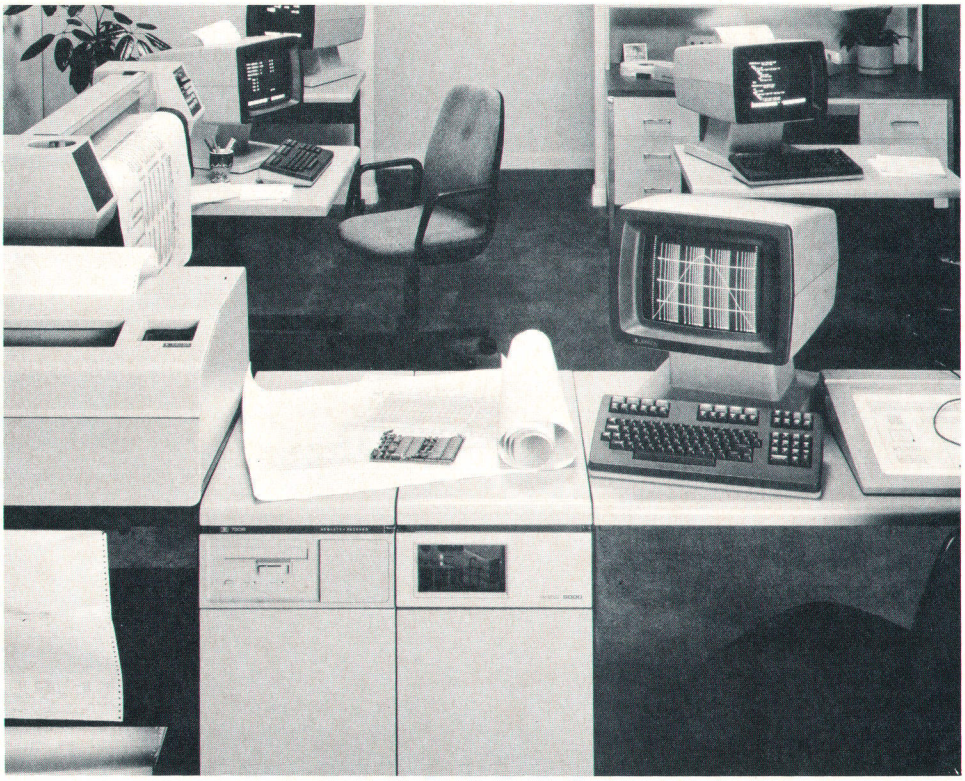


Fig. 2. *The design and styling of the Model 540 are compatible with other HP computer products, allowing it to fit in office configurations with an aesthetically pleasing appearance.*

All architectural blocks in the SPU are powered by an internal power supply module described in the article on page 24. This supply monitors its own outputs, controls fan speed, and shuts down if one of the doors is opened, the SPU's internal temperature is too high, or an output voltage is out of range. A signal denoting the cause of any shutdown is relayed to the system control module for display on its service panel.

Diagnostics

Our customers have always been able to identify any failed major system components such as the CPU, mainframe, disc, or printer. However, to do this they must run diagnostic programs, which require that a major part of the system be operating to give any information. Furthermore, a service engineer can obtain almost no information (let alone determine exactly what to replace), if the system processing unit is at fault. We wanted to take a new approach for the Model 530 and Model 540 SPUs, one that would enable a customer or service engineer to diagnose a problem down to the faulty module within the SPU and to identify any major failed external system components—even when almost nothing in the system is working.

To accomplish this, HP developed a diagnostic system that uses lower-level tests as a foundation upon which to build an increasingly comprehensive set of tests. These levels are the replaceable module self-test, the self-test supervisory code, and system diagnostics. If the system cannot proceed to the next level, the current level indicates why. Fig. 4 illustrates the various levels of diagnosis.

Replaceable Module Self-Tests. The replaceable module self-tests are the foundation for the self-test supervisory code and the system diagnostics. The module self-tests are low-level tests initiated by the modules on power-up and hardware or software request. We define a module to be any section of an SPU or peripheral that is field replaceable. Each of the finstrates in the Memory/Processor Module and each I/O card with a microprocessor performs a self-test. One fourth to one third of the microcode for the CPU and IOP finstrates is devoted to testing the respective IC. LED (light-emitting diode) indicators on the SPU's service panel show the results of these tests to the user. Each self-test is designed so that its results can also be read by higher-level diagnostics.

To ensure the most effective diagnosis, the self-test for each module is independent of the other self-tests so that (unless the power supply fails) a failure of a single module does not cause the other modules to fail their self-tests.

Self-Test Supervisory Code. This code is divided into two parts: the first part is resident in the system control module's loader ROM and is run as part of the power-up sequence, and the second part is resident in the power-up section of the operating system software.

To provide maximum usefulness, the loader test code tries to report status and fault information through multiple displays. Therefore, besides giving status and fault information via the LEDs on the SPU's service panel, it also displays a message on an attached terminal, if one is connected. The code first verifies the integrity of the internal I/O bus. Next it reads the self-test results for the I/O cards it may use for loading the operating system and for reporting status and fault information to the user. If there are no fatal failures such as a shorted internal I/O bus, the code performs several tests on the system control module, which include testing the real-time clock and the nonvolatile memory, and doing a checksum of the loader ROM itself. Consistent with our

self-test philosophy, if the loader ROM cannot load the operating system, it tells the user why.

The first part of the supervisory code, together with the replaceable module self-tests, constitutes the stand-alone self-test diagnostics. A user can check out the SPU and diagnose most problems without requiring any support peripherals. The second part of the supervisory code salvages "mapped out" RAM blocks (16K-bytes per block). These are blocks of RAM that failed the memory test performed by the memory controller's self-test. If only a few words of a block are bad, they are mapped out and the rest of the block is returned for use by the system. This part of the supervisory code also checks and reports to the user the results of the nonloader I/O card self-test.

System Diagnostics. These routines are written in high-level languages that can be called from the operating system. These routines can also initiate the power-up self-test of a module. If destructive testing such as disc writing is done, the user is warned of the effects of the testing before the test is started. This diagnostic code is on the main system disc and is used by production, repair areas, and service engineers.

These third-level test programs consist of two sets. There are verification programs for each peripheral, and for a minimum hardware system consisting of an SPU, a terminal, and a disc memory. These programs can be used by a customer or service engineer to verify the operation of the minimum system or a peripheral. The peripheral verification programs also test the interface card used with the peripheral.

The verification program for the minimum hardware system contains routines for checking the nonvolatile memory, the real-time clock, the key switches on the service panel, the terminal, and the disc memory. If any of these tests results in a failure, the terminal displays information detailed enough to isolate the cause to a field-replaceable module or peripheral.

Service Panel. The SPU's service panel is an important part of the diagnostic strategy. Its main purpose is to simplify testing and troubleshooting of the SPU. This panel allows fast isolation of faulty field-replaceable modules. It does this by providing a central location for displaying self-test results and power-up status information. It also provides easy viewing of this information from the front of the machine.

Status and fault information are indicated by LEDs on the service panel. During a normal, fault-free, self-test sequence, the service panel displays the sequence shown in Fig. 5. If a failure occurs, the sequence is aborted and the panel displays the fault condition. The service panel display can be matched with one of the fault indications listed in the service manual. Also listed in the service manual are procedures to fix each of the faults. Fig. 6 shows some possible fault indications and the procedures for determining what to check or replace to fix the faults.

The service panel also contains pushbuttons for initiating self-test, system reset, autostarting the system after a reset, and performing a memory core dump. The pushbutton for initiating self-test is self-latching. By latching this pushbutton, the service panel begins a continuous self-test mode that initiates both the hardware module self-tests and the self-test supervisory code. Testing continues until the pushbutton is released or until a failure is detected. The LED display indicates which field-replaceable module is faulty. If the SPU passes these tests, and if a disc memory with a loadable operating system is present, that operating system is loaded. The operating system then reads the latched **SELF-TEST** pushbutton and starts another self-test sequence.

The control for the service-panel display is located on the system control module. A microprocessor, called the service processor, gathers the results of the module self-tests and diagnostic information from the loader test code, and then indicates any failures by lighting the appropriate LED on the display. This service processor performs the following functions:

- Service processor self-test. The service processor does an internal ROM checksum test, an accumulator test, an internal RAM test, and a carry-bit test. This self-test is done at power-on, or at the start of a system self-test. If a failure is detected, the **SCM** (system control module) LED is lit on the service panel.
- Monitor processor stack self-test. During the system self-test, the service processor monitors the self-test signals from the Memory/Processor Module.
- Evaluation and display of processor stack self-test. Once the Memory/Processor Module self-test is complete, the

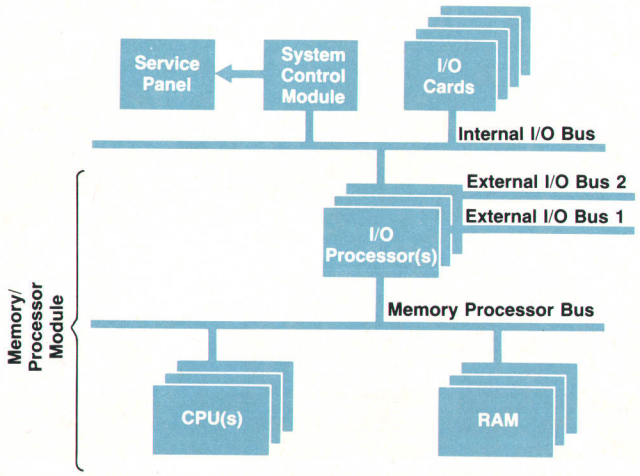


Fig. 3. *Internal architecture of the Model 530 and Model 540.*

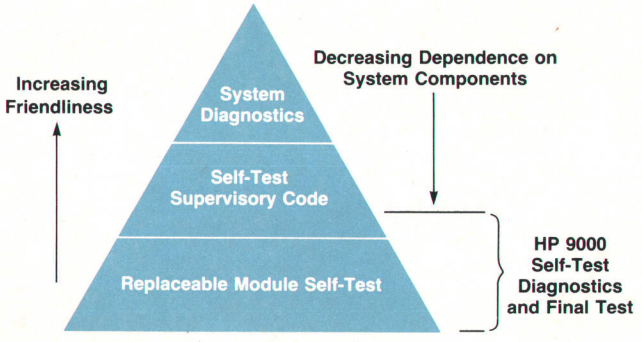


Fig. 4. *Diagram of the three diagnostic levels for the Model 530 and Model 540 System Processing Units.*

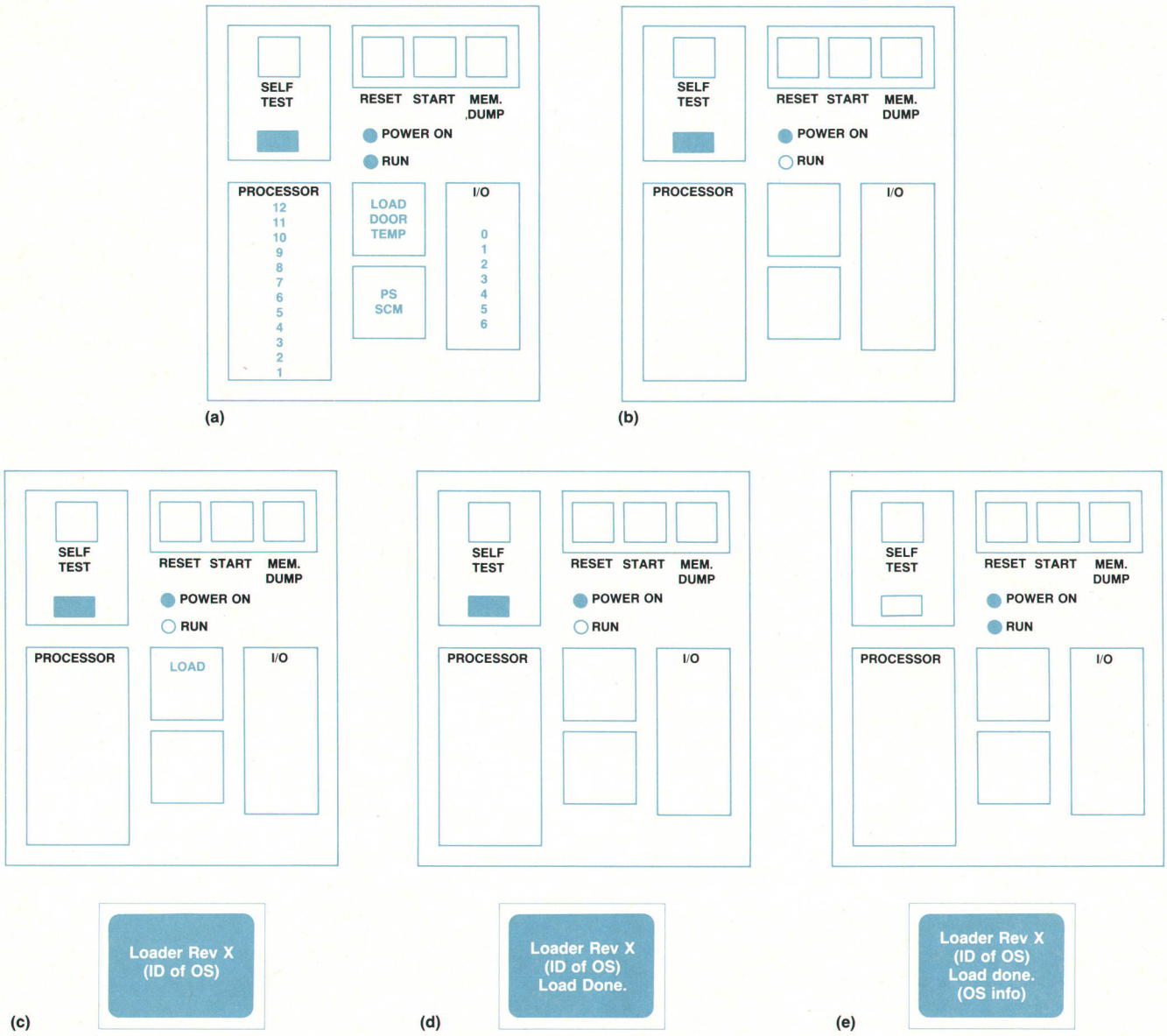


Fig. 5. *Service panel indications (color) and system display console messages during self-test sequence when the Model 530 and Model 540 are turned on. (a) Power on. (b) After one second. (c) After two seconds. (d) After seven seconds. (e) After 27 seconds.*

service processor can determine if any stack failures occurred. If there is a failure, the appropriate LED on the service panel is lit.

- Hard failure detection. If the system fails to power up (i.e., the loader code does not load), the service processor lights the appropriate LED on the service panel, giving the only indication why.

Some of the other circuitry provides control for the **POWER-FAIL** LED, the **HIGH TEMPERATURE** LED, and the **DOOR OPEN** LED. These failure modes cause the power supply to shut down except for the 16V supply that drives these LEDs.

Mechanical Design

The layout of the SPUs was determined by customer and service engineer needs. The design of the packaging components was based on production needs. To reduce manufacturing cost and design time, a large number of leveraged parts were used in the product design. Leveraging means using parts of existing designs instead of designing new hardware. In the SPUs the major leveraged components are the finstrates, Memory/Processor Module, power supply, I/O cards, HP's System-II rack-mount module design, and the cosmetic package used for the Model 540.

The only difference between the two SPUs is the outer package. The Model 540 is essentially the Model 530 mounted inside a cosmetically simple package to provide a pleasantly appealing look for an office environment. The cosmetic panels are the same as those used by HP's Disc Memory Division for their 79xx line of products.

When looking at the front of the Model 540, one can see two removable panels. Four self-test switches are exposed when the top panel is pulled off. The lower panel is removed by pulling near its top and pivoting about its bottom. The Model 530 can then be seen mounted inside on its side. When the Model 530 is ordered by itself, a removable cosmetic front panel is added. The next feature one might notice is a flat piece of sheet metal with six captive thumb screws. This sheet-metal part is used to reduce EMI. When this piece is removed, the hinged door of the Memory/Processor Module is visible. Loosening the two captive thumb screws on the Memory/Processor Module's door and opening it exposes the RAM finstrates. Below these finstrates, but not visible at this time, are the CPU and IOP finstrates.

Looking at the back of both models, one can see another door fastened with two captive thumb screws. Opening this door reveals a card cage with seven slots. This is where the I/O cards reside. If the second and third IOP finstrates were ordered with the SPU, two additional connectors will be located on the back. This is where the user can connect up to two HP 97098A I/O Expanders, each with eight additional I/O card slots.

On the Model 540, four screws must be unscrewed to remove the rear cosmetic panel. Then the procedure to service both SPUs is the same. A captive screw is unscrewed on the System-II rack-mount module to give the service engineer access to the power supply and the system control module board. The power supply is located in the center directly behind the Memory/Processor Module. The system control module board is located between the power supply and the I/O cards. Four screws must be unscrewed to remove either the supply or the board. The longest time it should take to diagnose a failure, replace a module, and put either SPU back together is 15 minutes.

Ease of production was a strong design consideration. Minimizing the number and types of screws used for assembly is an obvious help for production (and service). Using captive screws is also a big plus. Steel dowel pins align the SPU's motherboard with respect to the Memory/Processor Module and power supply. The pins allow the modules to plug directly into connectors on the motherboard even though the connectors cannot be seen when inserting the modules. A worst-case and 3.5σ tolerance analysis was used to ensure that parts would fit together in production. Whenever a screw passes through sheet metal, oversized holes are used to eliminate interference. Also, each module is thoroughly tested before the final assembly so that when the final turn-on test is run, there is a higher probability of successful operation.

Indication	Procedure
No service-panel LEDs on	Check/Replace: 1. AC power cord 2. Service panel cable 3. Power supply cable 4. Power supply assembly 5. AC module
DOOR	Close/Tighten: 1. I/O door 2. Processor stack door
TEMP	Check/Replace: 1. Ambient air temperature 2. Clogged filter/airflow blockage 3. Fans 4. Power supply assembly
PS	Check/Replace: 1. Power supply assembly 2. I/O cards 3. Finstrates 4. System control module 5. Motherboard I/O backplane
SCM	Check/Replace: System control module
PROCESSOR 10 Note: Any one of the 12 PROCESSOR LEDs may be on.	Check/Replace: Finstrate in slot 10
Note: One or more of the seven I/O LEDs may be on.	I/O 4 Check/Replace: 1. I/O card in slot 4 2. Peripheral device for slot 4 3. Interface cable for slot 4

Fig. 6. *Some examples of service panel indications when different faults are detected and the procedures to be followed to find the causes.*

Cooling

Three dc fans cool each SPU. These fans are also used in the Model 520 Computer, the desktop version of the Series 500. One fan cools the finstrates in the Memory/Processor Module. Another fan cools only the power supply, and the third cools the I/O cards and system control module. Since the fans, power supply and Memory/Processor Module were leveraged from the Model 520 design, the fan-speed control circuit was also leveraged. This means that in a normal office environment, the fans are run at a low speed to minimize noise. If ambient temperatures go up and the internal temperatures in the box become too high, the fans automatically switch to a higher speed to increase cooling. An even higher fan speed will be used if still more cooling is required. Temperatures of critical components are monitored to ensure that they run reliably.

Environmental Testing

All HP products are required to pass certain environmental tests. Therefore, each SPU must run reliably at 55°C. When placed in its shipping container, each SPU must survive free-fall drops from 460 mm on all six faces and four corners. However, the Model 540 is different from most HP products, because it is on casters and can be rolled around. Hence, the product can be abused in ways the normal environmental tests have no way of testing. Because of this, extra tests were run to make sure the Model 540's design would withstand such abuse.

Under normal use, the Model 540 may be pushed over rough surfaces or even accidentally run into a wall. Aggressive tests were set up to determine if the product would still continue to operate even under such abuse. The Model 540 was run off a ½-inch-thick piece of plywood, pushed in and out of elevators that were not lined up with the

floor, run into concrete walls at a fast walking speed, pushed into steel columns used to support the building, rotated about one set of wheels, and dropped from a height of 75 mm. An accelerometer was mounted inside the Model 540 to measure the accelerations exerted on the structure. Accelerations as high as 80g for 3 ms were observed. Despite this abuse, the product continued to function properly, and the only damage was some paint scratches, a few dents in the panels, and a few broken casters.

EMI Testing

Low susceptibility to radiated interference is linked, by reciprocity, to low radiated interference performance. For this and regulatory reasons, a host of electromagnetic compatibility (EMC) requirements dictated much of the design of the Model 530 and Model 540. In addition to meeting VDE and FCC radiated and conducted interference standards (VDE level A and B, FCC class A), design goals required that HP corporate standards for electromagnetic susceptibility also be met.

The Model 530 and Model 540 meet these challenges with a variety of techniques. On the printed circuit board level, ground planes are used to shield high-frequency signals and minimize current loop areas, a prime cause of crosstalk and interference. Along the same lines, logic common and shield (earth) ground are tied together at only one point on the SPU's motherboard, avoiding ground loop radiation and noise pickup problems. Sheet-metal shielding provides additional EMI protection as part of the SPU's mechanical design, not as an add-on feature. A typical metal shielding problem is the usual need for conductive gasketing to seal edges. Instead, the sheet-metal parts overlap and seal when they are bolted together, saving assembly time and complexity, and enhancing reliability. Gasketing is only used inside the Memory/Processor Module, the I/O panel door (for shield ground), and on an internal shielded ribbon cable. Finally, attention was also paid to all cutouts in the exterior sheet metal, because they can form slot antennas which radiate like dipoles. Slot length is kept to a minimum, since several small slots separated by metal are much better than one long slot of equivalent area.

Meeting all of the EMC objectives can, at times, present conflicting design choices. For example, Underwriter's Laboratories (UL) requires that all customer-accessible metal surfaces be able to sink a 30A current to shield ground. This might require some internal connections that would adversely affect the control of digital logic return currents, degrading EMI performance. The problem is further complicated by cabling and connection to other peripherals. The solution generally lies in diagramming the major current paths in the machine and looking for those with high impedance or large loop areas. Solutions are first evaluated as to how well they meet UL requirements and, if appropriate, how well they shield emissions by coupling RF energy to ground directly or capacitively.

Because of the complex nature of EMI generation and transmission, the only practical way of verifying regulatory compliance of designs is by testing to the appropriate standard. For high-frequency radiated emissions, this requires a 50-meter ground-plane surface (for repeatability and accuracy), a low-noise receiver or spectrum analyzer coupled with quasipeak (asymmetric averaging) and peak detectors having the required filter specifications,[5] and a set of antennas covering the range of 30 to 1000 MHz. Antenna correction factors are calculated and applied to the readings as they are taken. Since VDE specifies a quasipeak detector, final signal strength readings are based on it. It also offers better rejection of ambient noise than a peak detector. The total test system is heavily automated—an HP 9845 Computer controls the receiver through the HP-IB (IEEE 488), takes readings, sets frequencies, controls antenna height, and plots results. Operator intervention is only required for the initial manual scan, which determines the system's radiated frequencies, and to monitor successive automatic scans of different system orientations. This allows rapid examination of design alternatives.

Because development of the SPUs and some of their peripherals occurred in parallel, it was sometimes hard to isolate internal and external system problems to a particular product or assembly. Several tools are available to help in this process. Since any EMI frequency generated is usually a multiple of one of the system's fundamental clock frequencies, it is possible to isolate a problem frequency to a particular device directly if its clock frequency is unique. This can be done quickly by a simple computer program.

To test the operation of different I/O cables without having to hook up an associated peripheral (making problem isolation difficult), a "perfect peripheral box" was developed. This consists of a large copper sheet, acting as logic ground, mounted in a standard HP enclosure with a power cord connection to the back providing shield ground connection. Logic ground and shield ground can be optionally tied together inside the box. Different types of resistor-terminated cable connectors can be mounted such as HP-IB, RS-232-C/V.24, and general-purpose I/O. A high-speed (1M-byte/s) battery-powered handshake circuit can also be attached to the HP-IB connector for testing cable radiation.

After a problem is isolated to a particular device, it is necessary to determine where the offending RF is coming from on that device. This is done by means of "sniffer" probes, a few coiled turns of wire connected to a standard BNC connector on the end of a terminated coaxial cable. When connected to a spectrum analyzer, these directional probes help pinpoint the source of known problem frequencies. However, because of near-field effects, they do not accurately predict those frequencies that will be seen on the test range. Their sensitivity and precision are determined by the number and diameter of turns present.

Since neither the Model 530 nor the Model 540 contain internal I/O devices, and since many different peripheral systems had to be tested to verify regulatory compliance, a test setup did not always have a terminal or other input device for configuring the test software. Therefore, "smart" test software was developed that turns on a system, determines which of many different possible test peripherals is present, and exercises them accordingly, all without human intervention. With the addition of an input device, such as a digitizing tablet or terminal, various peripherals can be turned off and on under program control, helping to isolate problems quickly. This also saves much time when the system has to be powered down and back up

again quickly to verify problem frequencies.

Acknowledgments

These products represent the efforts of many people: Bob Brooks, Bob Montgomery, and Gary Seldner, part of the design team, Marcia Patterson, project coordinator, Gary Kaiser, marketing manager, Gary Thalman, service engineer, and Dave Luttrop, reliability engineer. Rick Donley and Steve Hodapp worked on the CE Handbook and Service Manual.

References

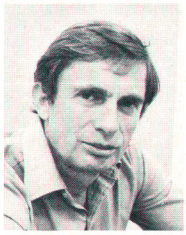
1. J. Beyers, et al, "A 32b VLSI Chip," *Digest of Technical Papers*, 1981 IEEE International Solid-State Circuits Conference, THAM 9.1.
2. J.W. Beyers, E.R. Zeller, and S.D. Seccombe, "VLSI Technology Packs 32-Bit Computer System into a Small Package," *Hewlett-Packard Journal*, Vol. 34, no. 8, August 1983.
3. A.K. Malhotra, et al, "Finstrate: A New Concept in VLSI Packaging," *ibid.*
4. J.M. Mikkelson, et al, "NMOS-III Process Technology," *ibid.*
5. *Specifications for Radio Interference Measurement Apparatus and Installations*, CISPR Publication 16, 1977.

Authors

May 1984

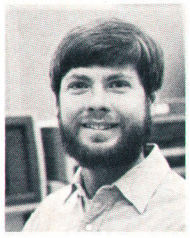
3 — 32-Bit Desktop Workstation

Paul F. Febvre



Born in Grenoble, France, Paul Febvre studied mechanical engineering at the Ecole d'Arts Et Metiers in Paris, receiving the MSME degree in 1959. He continued his studies at Colorado State University, earning an MSEE degree in 1963. He worked on R&D for an electroanesthesia company and came to HP when HP purchased the company in 1963. Paul did R&D for the 204C Oscillator, the 3403A RMS Voltmeter, and the 970A Multimeter. He managed R&D projects for HP's Grenoble Division in its early days, product design and production engineering for the HP 250 Computer, and product design for the HP 9000 Series 500 Computers. Paul is now responsible for product design and industrial design at HP's Fort Collins Systems Division. He is coauthor of two articles on the 204C Oscillator, one of which appeared in the HP Journal, and his work on the 970A Multimeter resulted in one patent. Paul served one year in the French Air Force and is a member of the International Electronics Packaging Society. He is married, has three children, lives in Fort Collins, Colorado, and enjoys organic gardening, cooking, and oil painting.

Ronald P. Dean

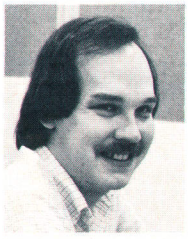


Ron Dean joined HP in 1977 after receiving a BSME degree from the University of Florida. He was production engineer for the tape transports used in the HP 9815, HP 9825, HP 9835, and HP 9845 Computers, and worked on the product design of the HP 9000 Model 520 Computer. He currently is working on new product design. Born in Dearborn, Michigan, he now lives in Fort Collins, Colorado. An active sports enthusiast, Ron enjoys softball, football, skiing, scuba diving, and aquatic activities.

Robert L. Brooks

With HP since 1966, Bob Brooks has contributed to a number of HP products—the 204C/D Oscillators, the HP 9845A Computer, and the HP 9000 Model 520 and 540 Computers—in the areas of product design and manufacturing. He currently is working on manufacturing processes for injection molded plastics. Born in Missoula, Montana, Bob served in the U.S. Navy for four years and then attended Montana State University, receiving a BSMT degree in 1966. He is married and has two children. He has a variety of interests ranging from keeping himself in shape to alpine skiing, sailing his 16-ft catamaran, working on HO and 1:8 scale live steam model railroads, and continuing the evolution of the home in Loveland, Colorado, that he and his wife designed.

Jack L. Burkman



Raised in western Montana, Jack Burkman studied mechanical engineering at Montana State University (BSME 1978). He then joined HP as an IC assembly engineer, later worked on the product design for the HP 9000 Series 500 Computers, and now is involved with future product design for HP 9000 enhancements. Jack lives in Fort Collins, Colorado, and serves as an arbitrator for the local Better Business Bureau. He is married, has two sons and a daughter, and enjoys spending time with his family, building black powder pistols, and restoring his old Triumph sports car.

Michael K. Bowen

A materials engineer and product designer for HP since 1979, Mike Bowen designed the die castings and miscellaneous parts for the HP 9000 Series 500 Computers. He holds a BSME degree awarded in 1978 by the University of California at Davis and is a member of the ASME. Mike was born in England, but considers Marysville, California his home. He is married (his wife is an assembly engineer at HP), has a daughter, and lives in Fort Collins, Colorado. Outside of work he enjoys bicycling, outdoor activities, skiing during the winter, and sailing and racing a Hobie Cat 16 during the summer.

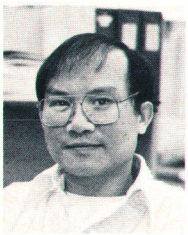
12 Color Graphics Display

Daniel G. Schmidt

With HP since 1981, Dan Schmidt supported production engineering for the HP 9915A Computer and worked on the 98760A Color Display for the HP 9000 Model 520 Computer. He currently is working on VLSI graphics subsystems. Dan is an author of a paper about a portable ROM simulator and holds a BSEE degree awarded by the University of Utah in 1981. Born in Salt Lake City, Utah, he now lives in Fort Collins, Colorado, with his wife and two children. Dan's outside interests include water and alpine skiing, travel, music, and home computer programming.

16 BASIC Graphics Subsystem

Xuan Bui

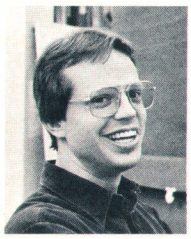


Joining HP in 1979, Xuan Bui worked on the graphics software for Series 500 BASIC and HP-UX commands. He currently is working on the operating system for HP-UX. A native of Hue, South Vietnam, he holds an MS degree in computer science (1979) from Louisiana State University. He is a member of the ACM and an author of a paper about numerical methods for solving differential equations. Married, he has one son, lives in Fort Collins, Colorado, and enjoys tennis and cross-country skiing.

Alan D. Ward

Alan Ward worked on the viewing transformations, output primitives, and device drivers for Series 500 BASIC graphics software before taking up his current assignment developing HP-UX graphics. With HP since 1979, he was born in Houston, Texas, and studied electrical engineering at the University of Texas (BS 1979). He is married, has four children, and lives in Fort Collins, Colorado. Outside of work, he likes camping, hiking, tennis, basketball, softball, and riding his motorcycle.

Kenneth W. Lewis



A native of Denver, Colorado, Ken Lewis studied mathematics at Western State College of Colorado (BA 1975) and computer science at the University of Colorado (MS 1979). He began work at HP in 1978 as a marketing application programmer for the HP 9845B Computer. He worked on the diagnostic programs for the HP 9845C, implemented the operating system interface and graphics device drivers for the BASIC version of the HP 9000 Model 520 Computer, and evaluated and tuned the performance of HP-UX for the Series 500. He currently is working on HP-UX graphics software. He is a member of the ACM, and before joining HP, did surveying and engineering for the Federal Highway Administration. He is married, lives in Fort Collins, Colorado, and enjoys hiking and skiing.

21 I/O Features

Gary D. Fritz

Before joining HP in 1979, Gary Fritz worked on rocket prelaunch test and monitoring for NASA. He wrote I/O code and operating system intrinsics for Series 500 BASIC, and more recently, taught HP service engineers about HP-UX. He currently is working on new workstation software. Born in Hawkeye, Iowa, Gary studied computer engineering at Iowa State University (BS 1979). He is single, lives in Fort Collins, Colorado, and has a variety of interests—skiing, bicycling, hiking, gardening, reading science fiction and fantasy, and playing frisbee.

Michael L. Kolesar

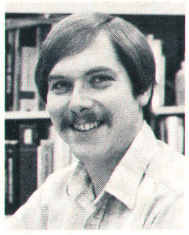
Mike Kolesar studied physics at Villanova University (BS 1968) and nuclear physics at Cornell University (MS 1971). He came to HP in 1974 with three years of experience in designing high-speed data acquisition systems for a synchrotron laboratory. Now a section manager responsible for graphics software and HP-UX commands and languages, he contributed to the architecture and microcode for the Series 500 CPU chip and managed some of the Series 500 software groups. He is coauthor of an award-winning paper on the Series 500 CPU architecture. Born in Chicago, Illinois, he is married, has three daughters, and now lives in Fort Collins, Colorado. He enjoys downhill and cross-country skiing, stereo music systems, photography, electronics, and hiking in the Rocky Mountains.

24 Compact Power Supply

Thomas O. Meyer

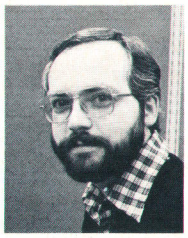
Born in Rapid City, South Dakota, Tom Meyer attended the South Dakota School of Mines and Technology, earning a BSEE degree in 1977. He then joined HP and contributed to the design of the memory and datacomm subsystems for the HP 250 Computer, wrote the assembly language code for the remote HP 250 (HP 2649D), designed and wrote the initial test code for the Series 500 power supply test station, and was responsible for the design of the primary board for the Series 500 power supply. Tom lives in Fort Collins, Colorado, and is interested in sailing, skiing, scuba diving, and touring Colorado's back roads on a motorcycle.

Howell R. Felsenthal



Howell Felsenthal joined HP in 1979 and began work designing servo control systems for a printer. He contributed to the development of the HP 9845 Computer, the Series 200 power supply, the 98780A Monochromatic Display, and the Series 500 power supply. He also performed environmental testing for the HP 9000 Series 500 Computers. Born in Ponca City, Oklahoma, Howell studied electrical engineering at the University of Oklahoma (BSEE 1977 and MSEE 1979). He is married, has two children, and lives in Fort Collins, Colorado. He enjoys skiing, playing softball, riding dirt bikes, and acting (he has been in two plays by the Loveland Community Theater).

Warren C. Pratt



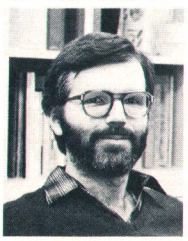
A native of Lexington, Kentucky, Warren Pratt studied electrical engineering at the University of Kentucky (BSEE 1974 and MSEE 1975) and the University of Illinois (PhDEE 1977). He then came to HP and designed analog display electronics for the HP 9845 Computer, managed a part of the Option 200 performance enhancement program for the HP 9845, and managed the subassembly integration, system electronics, and power supply development for the HP 9000 Series 500 Computers. He currently is section manager at HP's Fort Collins Systems Division. His work has resulted in one patent related to a deflection subsystem for a color raster-scan display. Warren is married, has a son and a daughter, and lives in Loveland, Colorado.

Jack L. Burkman

Author's biography appears elsewhere in this section.

31 32-Bit Processing Units

Robert E. Kuseski



Bob Kuseski has contributed to many HP products since coming to the company in 1969. His first project was the 9868A I/O Expander for the HP 9830A Computer. He designed the controller for the internal printer in the HP 9845A Computer (which resulted in a patent) and was responsible for converting

operating system and ROM software for the HP 9845B Computer. Bob also wrote microcode for the Option 200 enhancement to the HP 9845 and worked on the self-test philosophy and loader ROM test routines for the HP 9000 Series 500 Computers. He currently is working on new graphics hardware. Born in Columbus, Ohio, he served two years in the U.S. Army Signal Corps as a first lieutenant. Bob is a graduate of Ohio State University (BEE and MSEE, 1969), is married, has two children, and lives in Loveland, Colorado. He is active in church work and a member of Gideons International. Downhill and cross country skiing and playing table tennis occupy much of his leisure time.

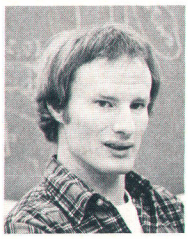
David Maitland

Dave Maitland's contributions have led to several patents and two papers related to integrated circuits and HP products. One of the papers received the Best Paper Award at the 1983 International Solid-State Circuits Conference. Dave was on the team that created HP's first desktop calculator, the HP 9100A, and was a project manager for the HP 9000 Series 500 Computers. An additional responsibility that he enjoys is recruiting for HP at his alma mater, the University of Illinois (BSEE 1964). He also holds a BA degree awarded by Rockford College in 1963. When he is not designing circuits in the R&D lab, Dave applies his engineering skills to the productivity of his farm near Fort Collins, Colorado. He is married, has two sons, and enjoys activities in the Colorado mountains and watching the Denver Broncos play football.

Larry J. Thayer

Born in Lancaster, Ohio, Larry Thayer attended Ohio State University and received a BSEE degree in 1978 and an MS degree in 1979. He then joined HP and designed the system control module and performed environmental testing for the HP 9000 Model 530 and Model 540 Computers. Larry is currently working on graphics hardware for future products. Living in Fort Collins, Colorado, he is vice president of his church congregation, is married, and is the proud father of a new son. Active in a variety of sports (baseball, softball, and alpine and Nordic skiing), he also enjoys hiking and photography.

Ronald D. Larson

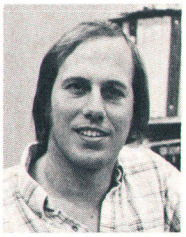


Ron Larson currently is working on graphics hardware for future HP products at HP's Fort Collins Systems Division. Joining HP in 1981, he worked on the development of the HP 9000 Model 530 and Model 540 Computers. A native of Pierre, South Dakota, Ron received a diploma in electrical technology from the North Dakota State School of Science in 1976 and a BSEE degree from South Dakota State University in 1981. He is single and lives in Fort Collins, Colorado. When not working, he enjoys hiking, alpine skiing, softball, and riding off-road motorcycles.

Kevin W. Allen

Kevin Allen studied mechanical engineering at the University of California at Davis (BSME 1978 and MSME 1979). He joined HP in 1979 and worked on product design for the HP 9000 Model 530 and Model 540 Computers before assuming his current responsibility as a process engineer for printed circuit board production. Kevin is a member of the ASME and has coauthored several articles on an electronic ski binding that he helped design. Born in Tucson, Arizona, he now lives in Fort Collins, Colorado, is married, and enjoys basketball, softball, and skiing.

Paul C. Christofanelli



Born in Kokomo, Indiana, Paul Christofanelli joined HP's Fort Collins Division in 1979 as a production engineer for the HP 9835 and HP 9845 Computers. He then moved to the R&D lab to work on system integration and EMI aspects of the HP 9000 Model 530 and Model 540 Computers. He is now concerned with new operating systems software. Paul studied electrical engineering at Arizona State University and was awarded a BSEE degree in 1976 and an MSEE degree in 1983. Single, he lives in Fort Collins, Colorado, and is interested in many different outdoor sports, among them water and alpine skiing and riding off-road motorcycles.

Hewlett-Packard Company, 3000 Hanover Street, Palo Alto, California 94304

Bulk Rate
U.S. Postage
Paid
Hewlett-Packard
Company

HEWLETT-PACKARD JOURNAL

MAY 1984 Volume 35 • Number 5

Technical Information from the Laboratories of Hewlett-Packard Company
Hewlett-Packard Company, 3000 Hanover Street
Palo Alto, California 94304 U.S.A.
Hewlett-Packard Central Mailing Department
Van Heuven Goedhartlaan 121
1181 KK Amstelveen, The Netherlands
Yokogawa-Hewlett-Packard Ltd., Suginami-Ku Tokyo 168 Japan
Hewlett-Packard (Canada) Ltd.
6877 Goreway Drive, Mississauga, Ontario L4V 1M8 Canada

CHANGE OF ADDRESS: To change your address or delete your name from our mailing list please send us your old address label. Send changes to Hewlett-Packard Journal, 3000 Hanover Street, Palo Alto, California 94304 U.S.A. Allow 60 days.

5953-8523